# Design and Characterization of a Compact and Broadband On-Chip Modified Three-Conductor Transmission Line Balun at G-Band


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***Abstract*—This paper studies the design and characterization of a millimeter-wave passive planar balun, which is implemented in the back end of line of a high-speed 130-nm SiGe BiCMOS technology. A modified three-conductor sub-quarter-wavelength transmission line based balun with an additional compensated transmission line is proposed to obtain a broad bandwidth, a compact area and reduced port imbalances. By means of a short termination approach and a deembedding method for reciprocal three-port component, measurement results show a 3-dB bandwidth from 140 GHz to 220 GHz with a minimum insertion loss of 0.7 dB. The amplitude imbalance is less than 0.8 dB and the phase error of differential output signals remains below 4° across the entire bandwidth. To the best knowledge of the authors, this proposed balun consumes the smallest area of 0.0038 mm$^2$ (excluding the pads) with the best phase balance at the G-band.**



***Index Terms*—Balun, deembedding, G-band, millimeter-wave, SiGe, sub-quarter-wavelength, three-conductor.**


## I. Introduction

The recent demand for high-resolution radar and imaging systems, as well as high data rate communication systems, is driving integrated circuit (IC) technology into the millimeter-wave (mm-wave) and sub-terahertz (sub-THz) frequency regions. With a significant development of advanced semiconductor processes, their high speed transistors offer a cut-off frequency $f_T$ and a maximum oscillation frequency $f_{max}$ up to several hundred gigahertz. Therefore, it enables the implementation of systems above 100 GHz for numerous mm-wave and sub-THz applications. In fact, a fully differential topology is preferable for these high performance systems due to its superior noise performance and output power. Consequently, baluns are essential for differential systems, to realize the conversion between balanced and unbalanced signals, especially for providing differential LO signals to balanced mixers and for driving differential amplifiers.

Generally, baluns are either active or passive according to system requirements. Active baluns can provide a finite gain at the cost of increased power consumption and a small area, whereas they suffer from noise and linearity limitations. In contrast, passive baluns introduce no additional noise and don't deteriorate the dynamic range, but they usually occupy more area. Due to the limited transistor gain and smaller wavelength towards mm-wave band, passive baluns are preferred when the corresponding area is comparable to that of active baluns, and the gain of active baluns is not needed for a particular system design. The broadside-coupled Marchand balun is the most commonly used passive balun, and has been implemented in many different technologies to achieve a broad bandwidth, lower losses and reduced amplitude/phase imbalances.

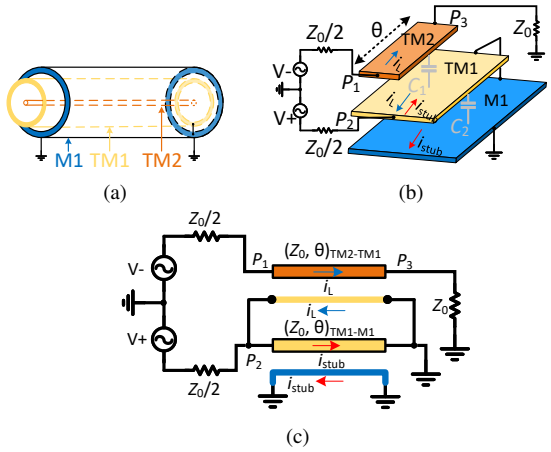


Fig. 1. (a) Three-conductor coaxial balun and its (b) planar three-conductor T-line in an IC technology and (c) its corresponding simplified circuit diagram.

In this paper, we present a planar modified balun based on the three-conductor transmission line (T-line) using an additional compensated T-line, to improve the bandwidth and port balance at G-band. To prove the concept, it is fabricated in the metal only back end of line (BEOL) run of 130-nm SiGe BiCMOS technology. Section II introduces the three-conductor sub-quarter-wavelength (SQWL) T-line balun, the shorted port termination technique based on the via-hole structures, and the deembedding method for reciprocal three-port devices. Sections III and IV present the analysis and design of the



The DOI of the final version is 10.1109/WAMICON64429.2025.11004106 .

balun and measurement results, respectively. A conclusion with a comparison to other G-band passive baluns is described in Section V.

## II. Theoretical Background

### A. Three-Conductor SQWL T-Line Balun

The three-conductor SQWL T-line balun concept is designed from a conventional three-conductor coaxial T-line and has been proposed as a planar balun in a multilayer monolithic microwave integrated circuit (MMIC) process by Park *et al.* [1], as shown in Fig. 1(a) and Fig. 1(b), respectively. In this implementation, the planar three-conductor T-line balun is implemented in three metal layers (TM2, TM1, and M1) by expanding the coaxial T-line to a planar form. Its single-ended port ($P_3$) on TM2 is connected to a load $Z_0$, while a pair of differential voltage sources with $Z_0/2$ is attached to the differential ports ($P_1$ and $P_2$ on TM2 and TM1, respectively). With the bottom metal M1 serving as the ground, the first top metal TM1 is substantially wider than the second top metal TM2. In Fig. 1(b), $C_1$ and $C_2$ represent the mutual capacitances between the coupling metal layers.

Fig. 1(c) shows the simplified circuit diagram representing the three-conductor T-line balun, which has an electrical length of $\theta < 90°$ at the desired frequency. Moreover, there are two independent T-lines in this three-conductor balun. One T-line with the characteristic impedance of $Z_{0,\text{TM2-TM1}}$ is formed between metal layers TM2 and TM1, which carries the current $i_\text{L}$. Another T-line with the characteristic impedance of $Z_{0,\text{TM1-M1}}$ is between the metal layer TM1 and the bottom layer M1, the corresponding current $i_\text{stub}$ goes through it. As reported in [2], the high value of $Z_{0,\text{TM1-M1}}$ increases the operation bandwidth at the expense of port imbalances. Consequently, the maximum bandwidth is achieved when the $Z_\text{ratio}$= $Z_{0,\text{TM1-M1}}/Z_{0,\text{TM2-TM1}}$ is 0.5 at the desired frequency.

### B. On-Chip Port Termination

The measurements of three- or more-port networks are becoming extremely hard as the frequencies approach the sub-THz region, since some required equipments are more expensive or not available (e.g. differential probes) at these high frequencies. In general, the commonly utilized approach to address this problem is to use two baluns in a back-to-back configuration, which changes the balun characterization to an on-chip two-port measurement [3]. However, using this method the port imbalances and insertion loss (IL) of individual path can not be measured. In this work, another approach from [4] is adopted, which is to perform two two-port measurements using an on-chip port termination technique at the differential output.

Passive components are typically fabricated in a low-cost metal-only run process, thus 50 Ω termination resistors are not available. According to [4], in order to achieve the on-chip port termination, a short structure consisting of a single via stack is implemented in a BEOL process. The corresponding lumped element model of the via stack comprises the inductance $L_\text{via}$ and resistance $R_\text{via}$ in parallel. At 180 GHz, it results in a total

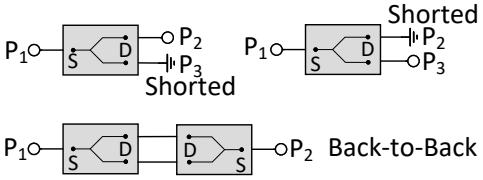


Fig. 2. Three two-port test configurations using only short terminations (top) and back-to-back structure of two three-port baluns (bottom).

$L_\text{via}$ of 1.8 pF and $R_\text{via}$ of 42.5 Ω by means of the calculations in [4]. Measurements demonstrate a real impedance close to 50 Ω, and a small remaining inductive component around 180 GHz.

### C. Deembedding Reciprocal Three-Port Devices

It is very challenging to determine the exact values for IC parameters, since environmental variables and process tolerances affect every sample. In addition, any S-parameter measurement will always have a limited accuracy. An appropriate set of two-port measurements can theoretically be used to extract the full n-port matrices (S, Y, or Z). To mitigate errors caused by an inaccurate load impedance and by measurement errors, a method for deembedding reciprocal three-port devices at mm-wave frequencies was developed in [5]. The method is performed on S-parameters only and is not affected by the actual load resistance. Theoretically, it is necessary to have a set of two-port test structures that simply include the device under test (DUT) and either an open or short reflection termination.

Fig. 2 shows three two-port test configurations using two shorted termination structures (port 2 shorted and port 3 shorted) and the back-to-back structure of two three-port baluns. By means of the analytic expressions from [5], an over-determined equation system can be obtained. The full S-parameter-matrix of the three-port DUT from the measurements can then be determined by solving it numerically.

## III. Design of Compensated Three-Conductor T-Line Balun

In this section, the design of a compensated three-conductor T-line balun is presented, which adopts the approach proposed in [6]. The proposed structure is a modified version of the balun utilizing an additional compensated T-line based on the three-conductor T-line SQWL balun, which is described in Section II-A. Fig. 3(a) illustrates the simplified circuit diagram of this balun with an open-circuit compensated T-line $TL_4$. In order to produce balanced ports, the T-lines $TL_2$ and $TL_3$ must have the same electrical length and characteristic impedance, which leads to $\theta_2 = \theta_3$ and $Z_2 = Z_3$. To achieve impedance matching and power dividing/combining, the electrical lengths and characteristic impedances of T-lines $TL_{\text{TM2-TM1}}$ and $TL_{\text{TM1-M1}}$ are optimized for the single-ended and differential port impedances. When the single-ended port is matched to the impedance $Z_1$ and the characteristic impedances of $TL_2$ and $TL_3$ are assigned to $0.5Z_1$. Using the

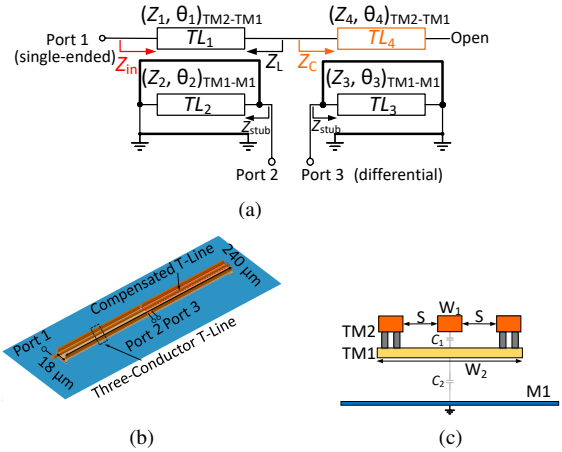


Fig. 3. (a) Simplified circuit diagram to represent the compensated three-conductor T-line balun. (b) 3-D layout view of this balun. (c) cross-section of this balun.

lossless T-line models, the theoretical S-parameters are given as

$$|\underline{S}_{11}| = \left| \frac{Z_{\text{in}} - Z_1}{Z_{\text{in}} + Z_1} \right| \tag{1}$$

$$S_{21} = -S_{31} = \frac{1}{\sqrt{2}} \sqrt{1 - \left| \frac{Z_{\text{in}} - Z_1}{Z_{\text{in}} + Z_1} \right|^2}. \tag{2}$$

Consequently, the return loss and insertion loss are related to the input impedance $Z_{\text{in}}$, which is partly determined by the $TL_4$. Compared to a traditional design, the use of the compensated $TL_4$ with the impedance of $Z_{\text{C}}$ results in an extended bandwidth by compensating the reactance. Additionally, $TL_4$ can be independently modified, including its characteristic impedance and the electrical length of this T-line. As reported in [6], the maximum bandwidth is obtained when the $Z_{\text{ratio}}$ equals 0.5 and the electrical lengths of all T-lines are set to about 60° at the desired frequency.

Fig. 3(b) demonstrates the three-dimensional (3-D) layout view of the proposed balun. In order to improve the IL, a grounded coplanar waveguide (GCPW) structure is used to implement the balun. The cross-section view of the balun is shown in Fig. 3(c), two sidewalls using the highest metal layer (TM2) are placed on the both sides of the $TL_1$ and $TL_4$ T-lines with a certain gap, which are connected to the second metal layer (TM1) through the vias. The lowest metal layer (M1) acts as a ground shield. All simulations of the designed balun were performed with the Keysight ADS EM solver.

## IV. Experimental Results and Deembedding

The BEOL process offers seven aluminium metal layers in total for the passive components. Among them, two top thick metals are best suited to realize high-quality mm-wave inductors and transmission lines, while the lower five thin metal layers are mostly used for interconnections. Fig. 4 depicts the micrographs of three test structures of the balun: two shorted baluns (port 2 and port 3) and one back-to-back connected two baluns. To further isolate the balun from nearby

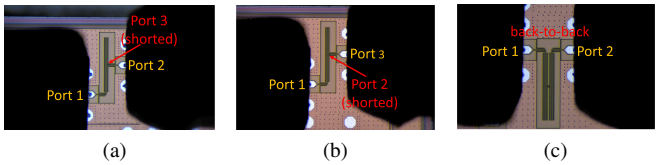


Fig. 4. Micrograph of the fabricated balun chip including three test structures with (a) shorted port 3, (b) shorted port 2 and (c) back-to-back connected two baluns (the area of balun = 0.0038 mm$^2$ without pads).

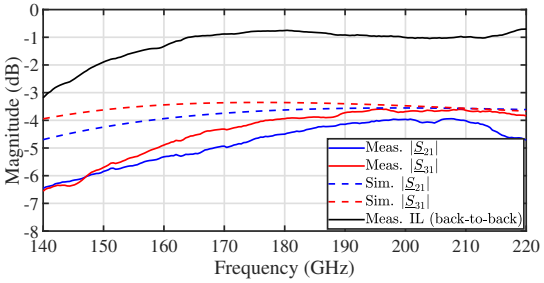


Fig. 5. Simulated and measured forward transmission coefficients of the proposed balun's differential ports 2 and 3 as well as the insertion loss of the two baluns in back-to-back structure.

components, it was embedded in a metal shield that expanding from bottom metal to the topmost metal layer. Excluding the chip pads, the core area of the balun occupies 0.0038 mm$^2$ (0.24 mm × 0.016 mm). In order to measure small signal characteristics, a network analyzer Rohde&Schwarz ZVA67 and two G-band frequency converter modules Rohde&Schwarz ZVA-Z220 were used. Additionally, two Cascade Infinity waveguide probes are directly connected to the chip pads. A line-reflect-reflect-match (LRRM) calibration algorithm was employed for S-parameter measurement.

All three test baluns are measured in a two-port network. The obtained two-port S-parameters data sets are solved numerically by means of an over-determined equation system, to deembed the complete S-parameters of the DUT from the measurements. The parasitics consist mainly of parallel capacitances and series inductances caused by the pad. These have been deembedded using an open-short (OS) method [7]. The two-step deembedding algorithm is analytically represented by:

$$Y_{\text{dut}} = \left[ (Y_{\text{meas}} - Y_{\text{open}})^{-1} - (Z_{\text{short}}^{-1} - Y_{\text{open}})^{-1} \right]^{-1} \tag{3}$$

where $Y_{\text{open}}$ is the admittance measured with the open pads and $Z_{\text{short}}$ is the impedance measured at the short pads, using the corresponding reference pad structures (not shown here). The derived S-parameters of the DUT are converted to Y-parameters $Y_{\text{dut}}$.

Fig. 5 presents the simulated and measured forward transmission coefficients of the differential port and the IL of two back-to-back baluns. Considering the 3-dB power dividing, the measured $|\underline{S}_{21}|$ and $|\underline{S}_{31}|$ demonstrate a minimum IL of 0.95 dB and 0.6 dB, respectively. The average IL shows a minimum of 0.7 dB by measuring two baluns in a back-to-back structure, thus a 3-dB bandwidth across the whole G-band from 140 GHz to 220 GHz is achieved. The shown

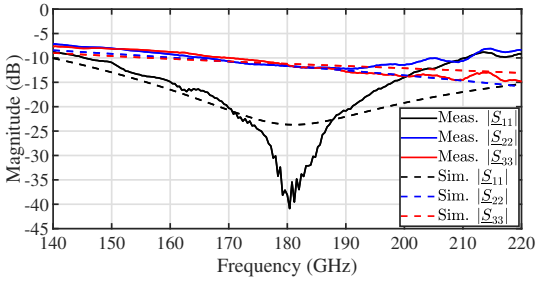


Fig. 6. Simulated and measured return losses of the proposed balun at single-ended and differential outputs.

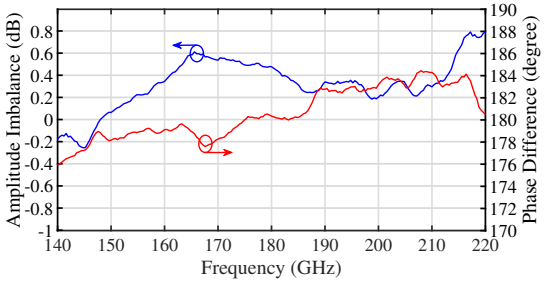


Fig. 7. Measured amplitude imbalance and phase difference characteristics of the proposed balun.

measurements indicate that the 3-dB bandwidth extends into the H-band, but due to limitations in the used measurement equipment we are not able to show this. The simulated and measured return losses at single-ended and differential outputs are shown in Fig. 6. The measured $|\underline{S}_{11}|$ is below -10 dB between 145 GHz and 198 GHz, while the measured $|\underline{S}_{22}|$ and $|\underline{S}_{33}|$ are below -8 dB over the whole D-band. It can be observed that the deembedded results align well with the simulations, which means that the ports are well-matched. Fig. 7 shows the measured phase and amplitude imbalance characteristics. Within the whole bandwidth of 140 GHz–220 GHz, the amplitude imbalance of the differential port is less than 0.8 dB, and the differential signal phase mismatch is less than 4°. Therefore, this balun has an excellent amplitude/phase balance and suppresses an undesired output common-mode signal over the entire bandwidth.

## V. Conclusion

In this work, a G-band on-chip modified balun based on the three-conductor sub-quarter-wavelength (SQWL) T-line with an additional compensated T-line was investigated and implemented. To enhance the bandwidth while maintaining the optimal port balance, the compensated T-line's characteristic impedance and electrical length were optimized, considering port impedance matching. Additionally, the balun is implemented utilizing a GCPW structure to achieve a compact area and low insertion loss. To prove the concept, the proposed balun is fabricated in a metal only BEOL of 130-nm SiGe BiCMOS technology. For small signal characterization at G-band, the three-port balun can only be measured by means of three test structures, which include two shorted configurations and one back-to-back structure. A deembedding method for reciprocal three-port devices is performed to obtain the deembedded complete S-parameter-matrix of the DUT from the only two-port network measurements. The measured minimum IL is 0.7 dB with a 3-dB bandwidth over the whole D-band. The balun achieves an amplitude imbalance of 0.8 dB and a phase error of 4°. Compared to the baluns shown in Table I, the proposed design has the best phase balance, while retaining comparable insertion loss and bandwidth. Furthermore, it requires the smallest chip area among them.

TABLE I
Comparison with other state-of-the-art mm-wave baluns.

| Ref. | **This work** | [8] | [4] | [5] | [5] |
|---|---|---|---|---|---|
| Tech. | **130 nm SiGe** | 130 nm SiGe | 130 nm SiGe | 130 nm SiGe | 130 nm SiGe |
| Topology | **Three-Conductor SQWL** | Marchand Edge-Coupled | Microstrip Lines | Marchand Stacked | Three Interacting Lines |
| Freq.$^{\hat{}}$ (GHz) | **140-220** | 200-325 | 140-220 | 140-220 | 140-220 |
| IL (dB) (min.-max.) | **0.7-3.2** | 2.3-3.3 | 0.32-3 | 0.6-2.2$^{*}$ | 0.1-1.5$^{*}$ |
| Amp. Error (dB) | **<0.8** | <1.5 | <1.5$^{*}$ | <1.2 | <0.6 |
| Phase Error (Deg) | **<4** | <10 | <5 | <5 | <5 |
| Size$^{\tilde{}}$ ($mm^2$) | **0.0038** | 0.015 | 0.05 | 0.0162 | 0.0064 |

$^{\hat{}}$: 3-dB bandwidth, $^{*}$: graphically estimated, $^{\tilde{}}$: without pads.

## Acknowledgment

This research was supported by the German Research Foundation (DFG) within the frame of the projects "TeraCaT" (under grant 506/45-1) and "TeraCaT II" (under grant 506/45-2).

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