Self-Organized Synchronization of Mutually Coupled Spatially Distributed 60-GHz PLLs

Christian Hoyer*¶, Franz Alwin Dürrwald*§, Florian Protze*, Jens Wagner*‡, Tilo Meister*, Frank Ellinger*‡
*Chair for Circuit Design and Network Theory, Technische Universität Dresden, Germany
‡Centre for Tactile Internet with Human-in-the-Loop (CeTI), Technische Universität Dresden, Germany
¶christian.hoyer1@tu-dresden.de, §franz_alwin.duerrwald@tu-dresden.de

***Abstract*—This study presents a significant advance in the field of self-organized synchronization using mutually delay-coupled phase-locked loops (PLLs) operating at 60 GHz. To confirm mutual synchronization, an integrated PLL architecture was designed in a 130 nm SiGe BiCMOS technology. Two nodes of these PLLs are mutually delay-coupled, and the effects of different division factors and time delays between the nodes are evaluated and compared with analytical predictions. An analysis of the accuracy of self-organized mutual synchronization is also performed. The study reveals that the division factor of the PLL significantly affects mutual synchronization behavior. The timing error has a standard deviation of 86.22 ps, while the peak-to-peak error is 590.95 ps.**

***Index Terms*—BiCMOS integrated circuits, couplings, delay effects, delays, frequency synchronization, oscillators, phase locked loops propagation delay, stability criteria, synchronization**

I. Introduction

Accurate synchronization of technical systems is crucial for enabling smooth operation and efficient coordination of processes and schedules. The accuracy of system synchronization is particularly important in application areas such as telecommunications, navigation, financial transactions, and control systems [1]–[3]. Various techniques are used to achieve high accuracy in synchronization among systems that need to be synchronized. These techniques can be grouped into common categories based on their centralization and hierarchy. In hierarchical systems, a precise clock often serves as the primary reference. The primary clock sends timing information to the secondary clocks. This method provides accurate and well-regulated synchronization, but is completely dependent on the quality and reliability of a primary clock. In non-hierarchical systems, the components have equivalent status and exchange time information with each other. This results in more resilient synchronization, but implementing these systems is more complex than using hierarchical approaches. Centralization refers to the existence of a central entity responsible for monitoring and controlling synchronization. Centralized systems rely on a single entity to coordinate. Decentralized systems distribute the responsibility of synchronization among components, thus making them self-organizing. Centralized hierarchical synchronization examples include clock trees or clock distribution networks. The Network Time Protocol (NTP) [4], [5] or the Precision Time Protocol (PTP) [6], [7] are well-known examples of a decentralized, hierarchical synchronization concept. In those concepts, time information are received by secondary clocks from multiple time server clocks at a higher hierarchy. Based on this approach, there are other protocols, such as White Rabbit [8]–[10], that allow even more precise synchronization.

A non-hierarchical decentralized approach is the self-organized mutual synchronization of clocks in a network with a flat hierarchy. This biological inspired method, based on the flashing behavior of fireflies [11], [12], provides a flexible and robust approach to synchronization. Unlike traditional hierarchical approaches, which distribute a precise time reference from a primary unit to other nodes, there is no such precise reference in this approach. This implies that such networks are not synchronized to a primary reference (e.g. GPS, UTC), but the clocks within the network are synchronized to each other. Understanding and implementing such a synchronization structure is particularly challenging due to the absence of a hierarchy. In fact, synchronization emerges from the self-organizing dynamics of the network and all nodes [13], [14].

The goal of this study is to prove this synchronization concept at millimeter-wave frequencies using phase-locked loops (PLLs) operating at 60 GHz. In contrast to previous research, this work uses a state-of-the-art architecture with fully integrated PLLs including phase frequency detectors and charge pumps. This concept has potentially benefits in several novel applications, in the area of advanced distributed sensor networks [15], [16], analog computing systems [17]–[20], and bio-inspired neural networks [21].

II. Model of Self-Organized Synchronization

The first ideas and models for self-organized synchronization were elaborated in the 1960s [22]. Based on these ideas, a linear model for mutual synchronization of spatially distributed oscillators was presented in [23], while [24] extended the analysis to include component nonlinearities. In recent years, theoretical studies of coupled oscillators have gained significant attention, providing deeper insights into the complex self-organizing dynamics of networks with time-delayed nonlinear interaction [25], [26]. The analysis of mutually coupled PLL networks has received significant attention in recent years, leading to a theoretical model that includes nonlinear coupling characteristics [27], [28]. This dynamical model is inspired by the Kuramoto model [29]

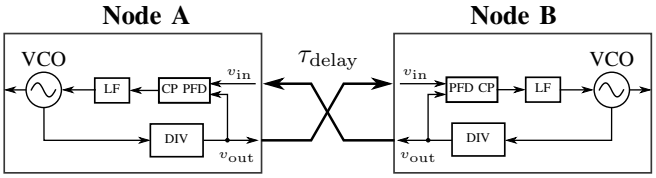


Fig. 1. Sketch of two PLL nodes A and B, which are mutually delay-coupled. Within this concept, the frequency-divided feedback signal is used similar to a reference signal for coupling with other PLL nodes.

for coupled harmonic oscillators and is adapted in a general way to networks of mutually delay-coupled PLL nodes. Within this model, any node k in the network is represented by the following set of implicit expressions [27], assuming that in a synchronized state all perturbations have decayed and that all nodes in the network are identical

$$\mathrm{N}\,\Omega_{\mathrm{NET}} = \omega_0 + \mathrm{K_{LF}}(0)\,\mathrm{K_{VCO}}\,\mathrm{K_{CP}} \times \frac{1}{\mathrm{E}_k}\sum_{i=1}^{\mathrm{M}} d_{ki}\,\mathrm{H_{PFD}}\left[-\Omega_{\mathrm{NET}}\,\tau_{\mathrm{delay},ki} \pm \Delta\varphi_{ki}\right]. \tag{1}$$

Where N is the frequency division factor of the PLL, Ω_{NET} is the divided angular output frequency of each node in the synchronized state, ω_0 the free-running closed-loop angular frequency, $\mathrm{K_{CP}}$ the gain of the charge pump (CP), $\mathrm{K_{LF}}(0)$ the steady state gain of the loop filter (LF), $\mathrm{K_{VCO}}$ the sensitivity of the voltage controlled oscillator (VCO) at the operating point, E_k the number of external inputs to a node k, M the number of PLL nodes in the network, d_{ki} the adjacency matrix parameter, which is either 1 or 0 depending on whether node k and i are coupled or not, $\mathrm{H_{PFD}}(\cdot)$ the normalized phase error transfer function of a phase frequency detector (PFD), $\tau_{\mathrm{delay},ki}$ the cross-coupling time delay between node i and k, and $\Delta\varphi_{ki}$ a constant phase difference between two nodes in a synchronized state. In case of two mutually coupled nodes, this constant phase difference will be either in phase ($\Delta\varphi_{ki} = 0$) or anti-phase ($\Delta\varphi_{ki} = \pi$). It depends on the properties of the phase detection circuitry [27], [28].

The network considered in this work consists of two nodes A and B, which are connected as shown in Fig. 1. Compared to the conventional way of using a PLL, the nodes are not unidirectionally connected to a reference. Instead, the frequency-divided feedback is used as an output signal for coupling to the input of another PLL node. The time delays between two nodes are equal in both directions. Therefore, the synchronized state of a PLL node depends on the incoming signal from another node as well as the phase difference induced by the time delay between nodes. A synchronized state is characterized by all coupled oscillator nodes in the network having identical frequencies Ω_{NET} and a constant phase difference between them. This can be determined by numerically solving (1). Whether these states are stable or not can be determined by analyzing their response to phase perturbations [14], [30].

This concept is self-organizing in the sense that the stationary frequencies and phase differences for synchronized states

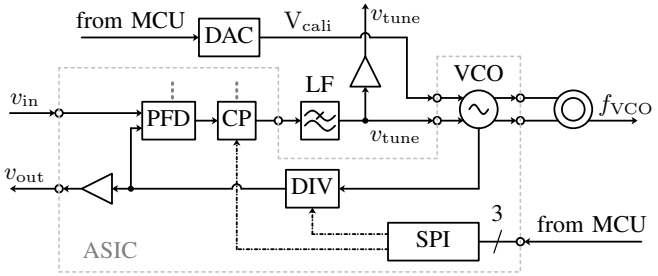


Fig. 2. Block diagram of a PLL node with phase frequency detector (PFD), charge pump (CP), loop filter (LF), voltage controlled oscillator (VCO), frequency divider (DIV) and serial peripheral interface (SPI). Only one input channel (PFD and CP) is used, all other channels are shown as gray dots.

are not externally determined. Rather, they organize themselves due to internal dynamics. To implement this concept successfully, it is necessary to have a thorough understanding of its underlying properties and limitations. Previous research has identified crucial aspects such as a critical delay, which determines the maximum delay between two nodes before the network becomes unstable [30]; for time delays where multiple stable synchronized states exists, the initial phase difference of the nodes affects the observable synchronized state [31]; and the phase noise between nodes is correlated and thus minimized compared to the free-running case [32]. Furthermore, recent studies have analyzed the effect of heterogeneous time delays between mutually coupled nodes [33]–[35].

III. Hardware Design and Measurement Setup

To study self-organized synchronization using mutual coupling, fully integrated PLL nodes are used. These application-specific integrated circuits (ASICs) are designed in a $130\,\mathrm{nm}$ SiGe BiCMOS technology with transit frequency f_{T} of $300\,\mathrm{GHz}$ and maximum frequency of oscillation f_{max} of $500\,\mathrm{GHz}$. An overview block diagram of the PLL node is given in Fig. 2. Each node consists of a VCO, presented in [36], operating in a frequency range around $60\,\mathrm{GHz}$. This VCO has two tuning voltage inputs $\mathrm{V_{cali}}$ and v_{tune}. The former is intended to be used as an input to set the closed-loop free-running frequency of the PLL using a digital-to-analog converter (DAC). This procedure is necessary to calibrate the respective nodes, ensuring that their operation ranges, particularly the lock ranges, overlap [37]. The input voltage with respect to the loop is v_{tune}, which can additionally be measured without affecting the loop using a buffer amplifier. This filtered output voltage originates from a CP and a PFD. To filter the signal, a passive lead-lag filter as LF with $-3\,\mathrm{dB}$ cut-off frequency of $413\,\mathrm{kHz}$ is used. The CP consists of seven current sources and sinks, with currents ranging from $250\,\mu\mathrm{A}$ to $4\,\mathrm{mA}$, and follows a traditional CP design [38]. A high-speed PFD drives this block, capable of detecting phase differences for signals up to the GHz range [39]. The feedback signal is the frequency-divided signal coming from the VCO. To allow mutual coupling, this signal is distributed as an output signal v_{out} to other nodes. An on-chip serial peripheral interface (SPI) allows external control of both the frequency divider (DIV) with division factor N and the CP with gain

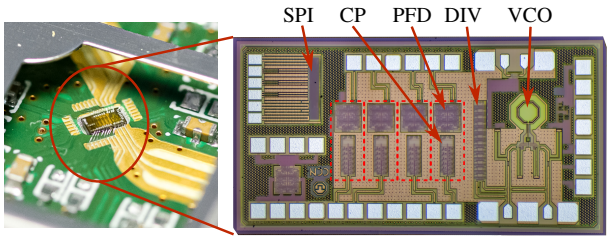


Fig. 3. The left side shows the assembled ASIC in a cavity on the top PCB, while on the right side is the ASIC with its main functional blocks. The input channels are denoted using dashed rectangles. The chip size is $965\,\mu\text{m} \times 1860\,\mu\text{m}$.

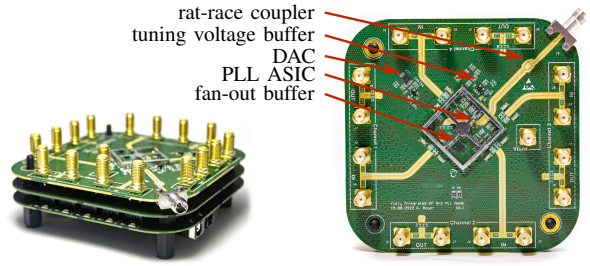


Fig. 4. On the left is the fully assembled PLL node with all stacked circuit boards. On the right is the top board for the complete functionality of the PLL node. The PCB size is $100\,\text{mm} \times 100\,\text{mm}$.

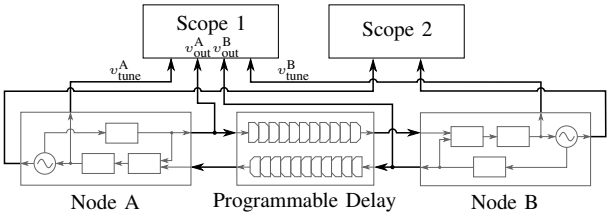


Fig. 5. The measurement setup comprises two mutually delay-coupled PLL nodes connected via a programmable delay. The divided frequency, phase difference between the nodes and the tuning voltages are measured with an oscilloscope (Scope 1), while the high-frequency waveforms are captured with a wideband oscilloscope (Scope 2).

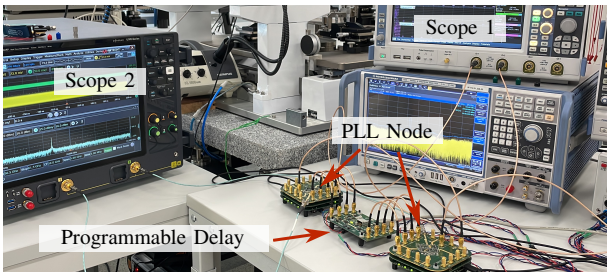


Fig. 6. Photograph of the measurement setup with two coupled PLL nodes connected via a programmable delay board. An additional spectrum analyzer is used during calibration using an automated test bench.

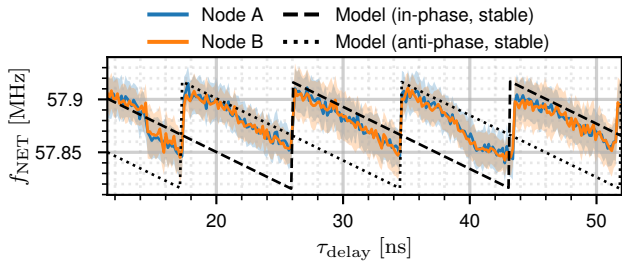
K_{CP}. The VCO's differential output signal, which operates at a frequency of $60\,\text{GHz}$, is converted to a single-ended signal via a rat-race coupler on the printed circuit board (PCB). To minimize the length of the bond wires for the high-frequency connection between ASIC and PCB, the ASIC is positioned in a cavity. With a maximum of four input channels consisting of PFD and CP, the ASIC can be used to connect more than one node. Fig. 3 shows a photo of the ASIC.

A photo of the PLL node is presented in Fig. 4. The node is composed of three custom PCBs: the top PCB contains the entire functionality of the PLL node, including the ASIC, LF, DAC, buffer amplifier, and a fan-out buffer for distributing the output signal to all output channels. The middle PCB serves as a redistribution layer for the power supply and contains the microcontroller (MCU) that controls the SPI. The lower circuit board is required for generating the power supply. Up to 10 supply rails can be set between $0\,\text{V}$ to $5\,\text{V}$ and up to $200\,\text{mA}$. The total power consumption of an entire PLL node is $2.35\,\text{W}$, while the PLL ASIC consumes only $375.8\,\text{mW}$. A significant portion of the power consumption is due to the DC termination of each input channel on the PCB and power supply generation.

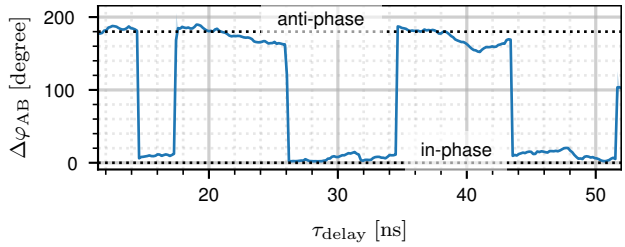
For the measurement of self-organized synchronization, two PLL nodes are mutually coupled via a programmable delay board [28], [32]. This board provides two channels, each equipped with four cascaded programmable delay chips, which allow setting the time delays $\tau_{\text{delay},ki}$ between the nodes. This delay can be set in $10\,\text{ps}$ increments between $11.4\,\text{ns}$ and $51.9\,\text{ns}$ for each channel. In addition, the delay board can be controlled via USB at runtime to adjust delays and enable coupling between the two nodes. To validate and characterize the synchronization and its states, the output waveforms v_{out} at the network level as well as the VCO output frequencies f_{VCO} of each node are recorded. Using the automated measurement function of the Scope 1, Rohde & Schwarz RTO 2044, it is possible to extract the frequency $f_{\text{NET}} = \text{N}\,\Omega_{\text{NET}}$ and the phase difference $\Delta\varphi_{ki}$ between the nodes. The spectrum of the two node VCOs is extracted from their high-frequency waveforms using a fast Fourier transform (FFT). The high-frequency waveforms are captured using the Keysight UXR0702 wideband oscilloscope (Scope 2). A sketch of the measurement concept is shown in Fig. 5 and a photo of the actual setup in the laboratory is shown in Fig. 6.

IV. Measurement

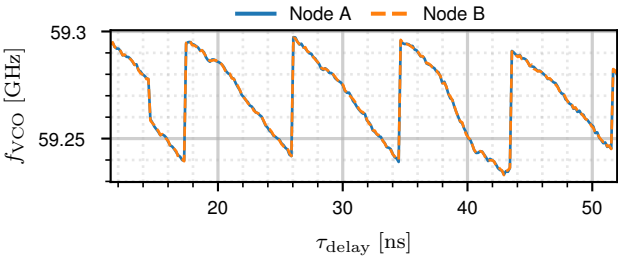
Self-organized synchronization is systematically analyzed in this work with respect to two main aspects. Firstly, the emergence of stable synchronized states using fully-integrated PLL nodes is validated for different time delays τ_{delay} by comparison to numerical results of (1). Secondly, the long-term stability of these states is quantitatively evaluated. For all measurements, the setup shown in Fig. 5 is used. Before any measurements were taken, all PLL nodes were calibrated to have nearly identical free-running frequencies using the additional input V_{cali} of the VCO via the DAC. Calibration is crucial to align the center frequencies and corresponding operating ranges of the PLLs. If this cannot be achieved, e.g. due to process, voltage and temperature (PVT) variations, correct and robust synchronization for all studied time delays cannot be ensured [37]. The time delay between nodes increases in a linear and symmetric manner, i.e. $\tau_{\text{delay,BA}} = \tau_{\text{delay,AB}} = \tau_{\text{delay}}$, for all measurements. During this parameter sweep, the nodes remain coupled.



(a) Network frequency f_{NET} of both nodes and model predictions.

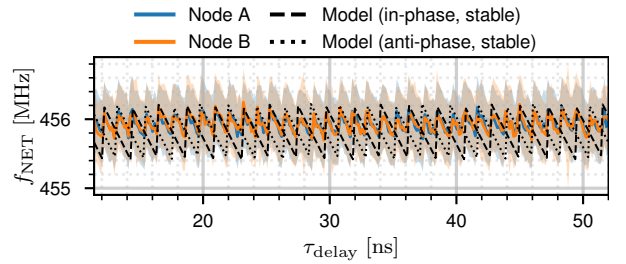


(b) Phase difference $\Delta\varphi_{\mathrm{AB}}$ between nodes.

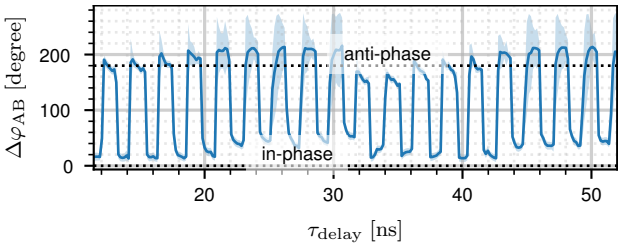


(c) Oscillator frequency f_{VCO} of both nodes.

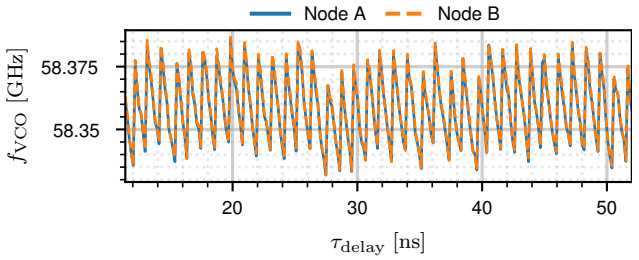
Fig. 7. Model results and measurements of synchronized states for two mutually coupled nodes as a function of the cross-coupling time delays τ_{delay}. The CP output current is set to 2.75 mA and a DIV of 1024. The standard deviation of the network frequency f_{NET} and the phase difference $\Delta\varphi_{\mathrm{AB}}$ between nodes for a minimum of 100 measurements is shown in shaded colors.



(a) Network frequency f_{NET} of both nodes and model predictions.



(b) Phase difference $\Delta\varphi_{\mathrm{AB}}$ between nodes.



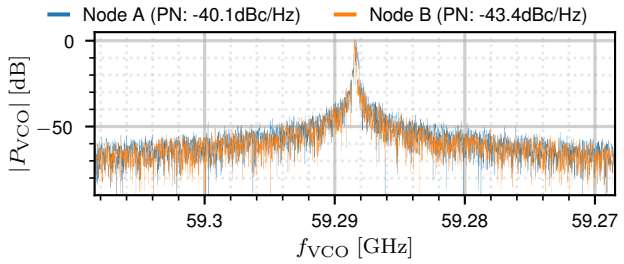
(c) Oscillator frequency f_{VCO} of both nodes.

Fig. 8. Model results and measurements of synchronized states for two mutually coupled nodes as a function of the cross-coupling time delays τ_{delay}. The CP output current is set to 2.75 mA and a DIV of 128. The standard deviation of the network frequency f_{NET} and the phase difference $\Delta\varphi_{\mathrm{AB}}$ between nodes for a minimum of 100 measurements is shown in shaded colors.

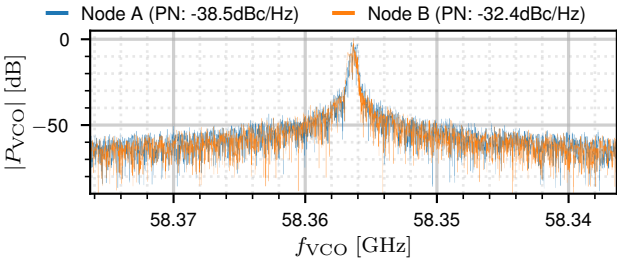
In the first case study, the output current of the charge pump is set to 2.75 mA and the frequency division factor is set to 1024. The results for synchronized states are presented in Fig. 7, showing stable synchronized states for each time delay studied. The numerical results for stable synchronized states with both in-phase and anti-phase phase difference between nodes agree with the measurements. However, it can be seen that the measurements always show a synchronized state with a higher frequency, i.e. the anti-phase synchronized state for a delay of e.g. 20 ns instead of an in-phase state. The maximum frequency difference in f_{NET} between both nodes is 59.46 kHz at a delay of 34.5 ns. The network frequency measured for all nodes, shown in Fig. 7(a), has a standard deviation from the mean of 37.7 kHz. The corresponding phase difference is shown in Fig. 7(b), the mean standard deviation of the phase difference is 2.83°. The peak VCO output frequencies f_{VCO} of both nodes are shown in Fig. 7(c). There is no significant difference between these frequencies, the maximum difference is 1.02 MHz at a delay of 34.5 ns.

For the second case study, shown in Fig. 8, the frequency is divided by a factor of 128, which leads to a higher network frequency f_{NET} of about 456 MHz. As in the previous case, only the synchronized state with a higher frequency can be observed. The numerical result and the measurement are in good agreement. The collective network frequency f_{NET} is shown in Fig. 8(a), where the maximum difference between the two nodes is 441.22 kHz at a delay of 41.5 ns. The corresponding phase difference is shown in Fig. 8(b). The mean standard deviation of the phase difference is 39.9°. Fig. 7(c) shows the peak VCO output frequencies f_{VCO} of both nodes. The maximum difference is 1.71 MHz at a delay of 44.8 ns.

The power spectral densities (PSD) of both node's high frequency VCO outputs for all studied cases are shown in Fig. 9. The resolution bandwidth of the FFT function on Scope 2 is 7.63 kHz. In the first analyzed case, depicted in Fig. 9(a), both nodes have identical center frequencies of 59.288 GHz. The phase noise (PN) at a distance of 1 MHz from the carrier is between −40.1 dBc/Hz and −43.4 dBc/Hz. For the second scenario, the center frequencies remain identical at 58.356 GHz and the PN at an offset of 1 MHz is −38.5 dBc/Hz for node A and −32.4 dBc/Hz for node B,



(a) PSD of the VCO output at a frequency f_{VCO} of 59.288 GHz for a delay of τ_{delay} of 50 ns and for the case shown in Fig. 7.



(b) PSD of the VCO output at a frequency f_{VCO} of 58.356 GHz for a delay of τ_{delay} of 51.2 ns and for the case shown in Fig. 8.

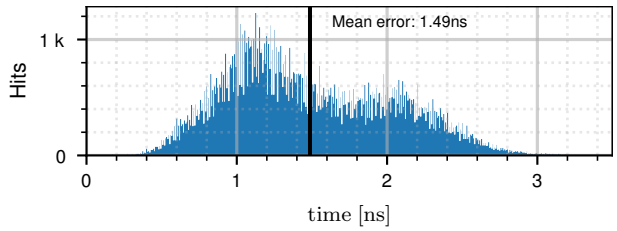
Fig. 9. Measured normalized power spectral densities (PSD) output and phase noise level (PN) at an offset of 1 MHz from the carrier for both mutually coupled PLL nodes for both studied cases.

as shown in Fig. 9(b).

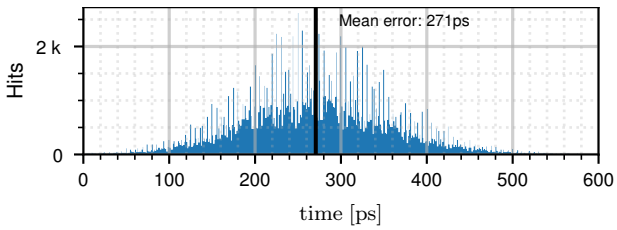
To quantify the accuracy of time synchronization, the v_{out} waveforms of the frequency-divided VCO signals are considered. By using the automatic measurement function of Scope 1, the time difference between two rising edges of v_{out} of both nodes is measured. For ideal synchronization in an in-phase synchronized state, it is expected to be zero in any case [40], but due to noise these waveforms are subject to jitter. Timing jitter is analyzed using histograms. Fig. 10 shows the results of this analysis. The case of a division factor of 1028 is shown in Fig. 7 and 128 in Fig. 8. In the first case, the time delay τ_{delay} is equivalent to a distance of 9.99 m at a speed of $2/3$ of the speed of light, which is a typical value for coaxial cables. For this case, the mean error is 1.49 ns, the standard deviation is 545 ps, and the peak-to-peak error is 3.45 ns. The peak-to-peak error is the difference between the minimum and maximum measured values. For the second scenario, which corresponds to a distance of 10.24 m, the mean error is 270.69 ps, the standard deviation is 86.22 ps, and the peak-to-peak error is 590.95 ps.

V. Conclusion

The presented findings in this study provide clear evidence supporting the feasibility of self-organized synchronization through the use of mutually delay-coupled phase-locked loops (PLLs). To verify the theoretical predictions, a PLL architecture was designed in a 130 nm SiGe BiCMOS technology. This architecture includes a frequency divider and a voltage-controlled oscillator operating at 60 GHz. It allows for coupling with multiple other PLL nodes using phase-frequency detectors and charge pumps. The accuracy



(a) Histogram for τ_{delay} of 50 ns and in the case of N of 1024.



(b) Histogram for τ_{delay} of 51.2 ns and in the case of N of 128.

Fig. 10. Timing jitter between waveforms of network frequency f_{NET} for two coupled nodes for 200 k measurements for both cases studied.

TABLE I
Comparison with state-of-the-art synchronization concepts.

Ref.	Distance	Mean error	Standard deviation	Peak-to-peak error
[10]	1.5 m	143.7 ps	23.9 ps	176.7 ps
[41]	-	274.6 ps	4.28 ns	28 ns
[7]	100 m	50.4 ps	176 ps	1.21 ns
[6]	100 m	70.7 ps	64 ps	510 ps
This	9.99 m	1.487 ns	545.06 ps	3.448 ns
This	10.24 m	270.69 ps	86.22 ps	590.95 ps

measurements shown in Table I underscore the potential of mutual PLL synchronization as a robust and reliable method, especially when using higher coupling signal frequencies. In the scenarios studied, the peak-to-peak error decreased from 3.45 ns at a division factor of 1024 to 591 ps at a division factor of 128. Relating these numbers to the period of the signal used for coupling, the relative peak-to-peak error is 2.13 or 2.21. In effect, this means that the relative error is not reduced due to changes in the cross-coupling frequency, but the absolute error is. Although further improvements are possible, these results highlight the importance of ongoing research in self-organizing synchronization, especially in the context of precise timing measurements, to fully understand the complex nonlinear dynamics and interactions involved.

Acknowledgment

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