

A 5.8 dBm 55.2–67 GHz Frequency Sixtupler with 37 dB Conversion Gain in 130-nm SiGe BiCMOS

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Abstract—This paper presents a V-band frequency sixtupler in 130-nm SiGe BiCMOS, achieving a high conversion gain (CG) and harmonic suppression (HS). The design cascades a class-A differential frequency tripler with a bandpass filter followed by a driver amplifier for third harmonic extraction and a bootstrapped Gilbert-cell based frequency doubler to generate the sixth harmonic. An active balun ensures balanced operation, while an asymmetric coupled line balun suppresses undesired harmonics at the single-ended output. Measured results demonstrate a peak output power of 5.8 dBm at 61.2 GHz with 37 dB CG and 4.2% total efficiency, consuming 90 mW dc power. A 3-dB bandwidth (BW) from 55.2 GHz to 67 GHz is achieved with at least 35 dB HS across the whole band. To the best knowledge of the authors, this work achieves the highest reported CG for V-band frequency multipliers.

Index Terms—SiGe BiCMOS, V-band, signal generation, frequency multiplier, conversion gain, harmonic suppression

I. INTRODUCTION

The growing demand for millimeter-wave (mm-wave) systems, such as 6G, satellite communications, and high-resolution radar, necessitates high-performance local oscillators (LOs) capable of generating spectrally pure signals at V-band frequencies (40–75 GHz). However, generating LO signals with high spectral purity and low phase noise at these frequencies remains a challenge [1]. Traditional voltage-controlled oscillators (VCOs) with phase-locked loops (PLLs) suffer from a limited efficiency, narrow locking ranges, and high phase noise at these frequencies.

A viable alternative approach that circumvents these challenges is the use of low-frequency sources in a cascade with frequency multipliers, to achieve high-frequency LO signals. Prior works demonstrate multipliers [2]–[4] for mm-wave applications, however achieving high output power with robust HS remains challenging. For instance, [3] reports an E-band frequency sixtupler with high spectral purity, yet limited CG of 8.5 dB. This work presents a V-band frequency sixtupler in 130-nm SiGe BiCMOS, combining a harmonic-based frequency tripler [5] and a bootstrapped Gilbert-cell based frequency doubler [6]. The frequency tripler employs a class-A cascode amplifier with a bandpass filter for third harmonic extraction, while the frequency doubler enhances BW and CG through a Gilbert-cell topology. An active balun ensures balanced operation, and an asymmetric coupled line balun [7] suppresses undesired harmonics at the single-ended output.

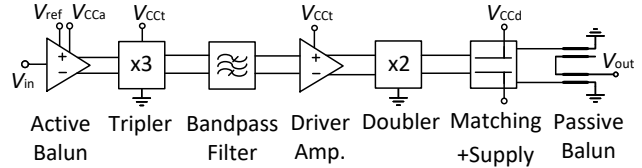


Fig. 1. Block diagram of the proposed V-band frequency sixtupler.

II. CIRCUIT DESIGN AND IMPLEMENTATION

The block diagram of the proposed frequency sixtupler is depicted in Fig. 1. The circuit employs a cascaded chain: an active balun converts a single-ended 10 GHz input to differential signals, followed by a harmonic-based frequency tripler with a bandpass filter, a driver amplifier, and a bootstrapped Gilbert-cell based frequency doubler, which generates the desired 60 GHz signal. An asymmetric coupled line balun at the output ensures single-ended operation and HS.

As illustrated in Fig. 2, an active balun converts single-ended 10 GHz inputs to balanced differential signals for the frequency tripler, using a common-base stage (T_3) for 50 Ω broadband matching. Its cascode differential pair (T_4 – T_5) generates outputs with minimal phase and amplitude imbalances, where T_5 's ac-ground connection ensures symmetry [5]. Optimized for both signal conversion and gain enhancement, this design improves the system's performance by delivering precise phase-matched inputs while suppressing harmonics. This stage pre-amplifies the signal while enabling balanced driving for nonlinear harmonic generation in the subsequent frequency tripler.

The next stage, as shown in Fig. 2, is a harmonic-based frequency tripler [5], leveraging a class-A cascode differential amplifier (T_9 – T_{12}) overdriven into nonlinear saturation to generate odd harmonics. Its resonant load network (C_C and TL_C) extracts the third harmonic (30 GHz) and enables high CG and suppression of unwanted harmonics via impedance peaking. A subsequent bandpass filter (C_F and TL_F) rejects the fundamental frequency, ensuring high spectral purity delivered to the next stage. A driver amplifier (T_{13} – T_{16}) then boosts the tripled signal to compensate for inter-stage losses.

The Gilbert-cell based frequency doubler from [6] shown in Fig. 2 employs a differential transconductance (g_m) pair (T_{23} – T_{24}) and switching quad (T_{19} – T_{22}) for second harmonic

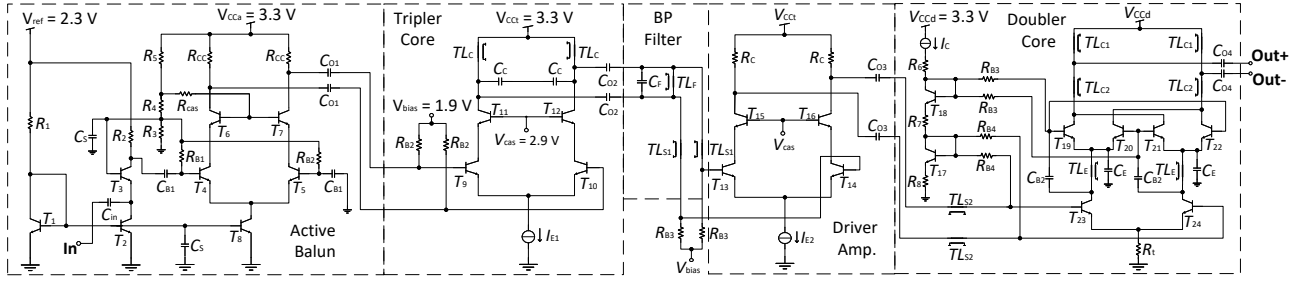


Fig. 2. Schematic of the proposed frequency sextupler chain.

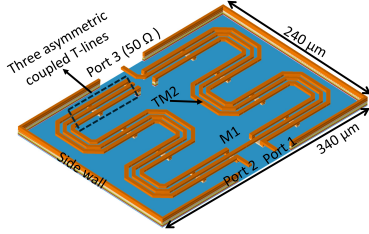


Fig. 3. 3D view of the designed three asymmetric coupled lines balun.

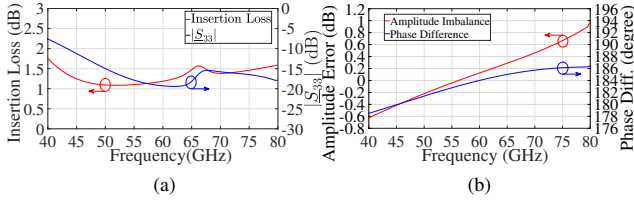


Fig. 4. Simulated (a) insertion loss and output reflection coefficient and (b) amplitude error and phase difference characteristics of the proposed balun.

generation. Its bootstrapped architecture directly connects the switching quad inputs to the g_m pair collectors, pre-amplifying the LO signal before it drives the switching transistors. This approach results in a superior CG compared to conventional Gilbert-cell implementations. At the RF input, two phase-shifting transmission lines (TL_E) optimize the switching quad voltage, which improves both output power and conversion efficiency. Additionally, shunt capacitors (C_E) suppress spurious harmonics by grounding them. A tail resistor (R_t) minimizes higher-order even harmonics from self-mixing and leakage.

For measurement compatibility, the output differential-to-single-ended conversion employs a three asymmetric coupled lines balun from [7] using the topmost metal layer TM2 (3 μm) for low-loss transmission and metal layer M1 for ground shielding. The 3D view of the balun is illustrated in Fig. 3. By leveraging three asymmetric coupled lines, where the inner line forms a $\lambda/2$ open stub, and the outer lines act as $\lambda/4$ short stubs, the odd-mode capacitances were enhanced, achieving a balanced even/odd-mode phase velocities and reduced phase/amplitude imbalances across a wide frequency range. Using a lower metal layer (TM1) with vias to connect short stubs in one arm further reduces phase errors. According to EM-simulations, the balun demonstrates a -10-dB $|S_{33}|$ BW from 43 GHz to 80 GHz, with an insertion loss of 1.1–

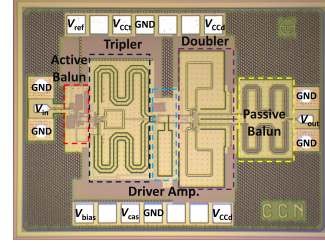


Fig. 5. Micrograph of the frequency sextupler chip. The chip area (including pads) is 1.3 mm \times 1 mm.

1.7 dB in Fig. 4(a). A phase imbalance under 6 degrees and an amplitude imbalance less than 1 dB are shown in Fig. 4(b).

III. EXPERIMENTAL RESULTS

To prove the concept, the proposed frequency sextupler was fabricated in 130-nm SiGe BiCMOS technology featuring transistors with maximum f_T/f_{max} of 300 GHz/500 GHz [8]. As shown in Fig. 5, the complete circuit occupies 1.3 mm² including pads, with a total dc power of 90 mW. On-wafer measurements were conducted using a Rohde & Schwarz ZVA-67 network analyzer, Keysight E8257D signal generator and Rohde & Schwarz FSW-67 spectrum analyzer.

The small-signal characteristics are shown in Fig. 6(a), it shows the measured and simulated $|S_{11}|$ and $|S_{22}|$, which proves good agreements with simulations. The $|S_{11}|$ remained below -10 dB from 5–25 GHz, while the $|S_{22}|$ stayed under -10 dB from 56–64 GHz, ensuring efficient power transfer at the sixth harmonic. For large-signal characterization, the measured output power at the 2nd through 6th harmonics and CG as a function of the input power at 10.2 GHz input frequency are shown in Fig. 6(b). The output power at fundamental frequency is not shown here as the values are significantly smaller than the noise floor of the device. The circuit reveals a saturated 6th output power of 5.8 dBm and achieves a peak CG of 37 dB. Fig. 7(a) demonstrates the measured saturated output power for an input power of -15 dBm versus input frequency. A maximum 6th harmonic output power of 5.8 dBm at the frequency of 61.2 GHz is achieved, which results in a total efficiency $\eta_{\text{tot}} = P_{\text{out}}/(P_{\text{DC}} + P_{\text{in}})$ of 4.2 % at 90 mW of dc power. It can be observed that a 3-dB BW of 11.8 GHz from 55.2–67 GHz is measured. Additionally, the measured output power at the 6th harmonic and CG fit the simulated values well. The measured suppression of the 2nd through 5th

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART OF HIGHER-ORDER FREQUENCY MULTIPLIERS OPERATING BETWEEN 33 GHz AND 71 GHz

Ref.	This work	[2]	[9]	[3]	[10]	[4]	[1]
Technology	130nm SiGe BiCMOS	28nm CMOS	22nm FD-SOI	55nm SiGe BiCMOS	90nm CMOS	130nm SiGe	65nm CMOS
MF ($\times N$)	$\times 6$	$\times 4$	$\times 4$	$\times 6$	$\times 6$	$\times 8$	$\times 8$
Topology [§]	AB+FT+DA+FD	FD+DA+FD+Buffer	FD+FD+DA	FT+FD+Buffer	FT+ILO+FD	FD+DA+FD+DA+FD+DA	DA+FD+FD+DA+FD+DA
Output frequency* (GHz)	55.2–67	52–65	54.9–65.7	65.9–78.6	33.6–40	56–71	46.4–52
Max. P_{out} (dBm)	5.8	-1.8	-10	5.6	-1	13.5	-1.8
Max. CG (dB)	37	-1.8	-19 [†]	8.5	-1	17	22.2 [∇]
HS (dB)	>35	>35	>22.5	>38.5	>15.96 [†]	>40	>37.6
Total efficiency η_{tot} (%)	4.2	1.6	0.45	5.66	9 [∇]	5.45 [∇]	1.2 [∇]
P_{DC} (mW)	90	49	12	63.1	7.72	410	55
Chip size (mm ²)	1.3	0.07 [^]	0.2	1.17	0.49	1.35	0.92

*: 3-dB bandwidth, [^]: only core area, [†]: graphically estimated, [∇]: calculated, [§]: AB: active balun; FT: frequency tripler; FD: frequency doubler; DA: driver amplifier; ILO: injection-locked oscillator.

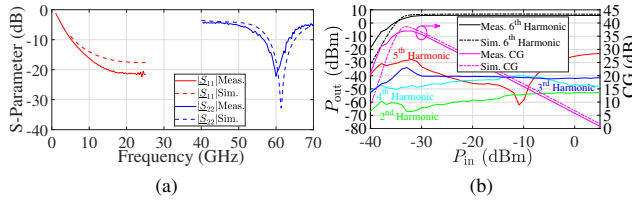


Fig. 6. Measured (solid lines)/simulated (dashed lines) (a) reflection coefficients at the input and output; (b) output power at 2nd, 3rd, 4th, 5th and 6th harmonics and CG versus the input power for $f_{in} = 10.2$ GHz.

harmonics is illustrated in Fig. 7(b). Over the whole 3-dB BW of the 6th harmonic, which is centered at around 61.2 GHz, the suppression of any harmonic power exceeds 35 dB.

IV. CONCLUSION

In this work, a high-performance V-band frequency sextupler implemented in 130-nm SiGe BiCMOS is investigated and characterized. The proposed design integrates a harmonic-based frequency tripler and a bootstrapped Gilbert-cell based frequency doubler in a cascaded architecture, enhanced by an active balun for balanced signal conversion, an inter-stage amplifier with a bandpass filter for power boosting and HS, and an asymmetric coupled line balun for single-ended output matching. The circuit delivers a peak output power of 5.8 dBm at 61.2 GHz and achieves a CG of 37 dB, while maintaining a high HS of at least 35 dB over a 3-dB BW from 55.2 GHz to 67 GHz. The total efficiency and dc power consumption of the frequency sextupler are 4.2% and 90 mW, respectively. Table I compares the proposed frequency sextupler to the state-of-the-art of higher-order frequency multipliers operating between 33 GHz and 71 GHz. The proposed frequency sextupler provides the highest CG with a competitive total efficiency and excellent suppression of the undesired harmonics.

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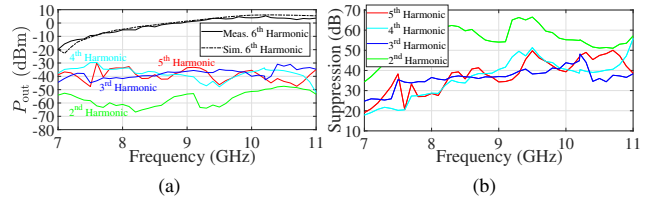


Fig. 7. Measured (solid lines)/simulated (dashed lines) (a) output power at 2nd, 3rd, 4th, 5th and 6th harmonics and (b) spurious harmonic suppression versus input frequency for $P_{in} = -15$ dBm.

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