Integration Technology Development of Chip-Antenna Interface for Short Range mmWave Wireless Communication

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***Abstract*—Given the increasing demand for highly integrated, high-performance packaging, this paper investigates packaging technologies for embedding chips and antennas in high-frequency applications. We propose a fan-out wafer-level packaging (FOWLP) approach that utilizes a semi-additive redistribution layer (RDL) to route high-frequency signals from embedded dies to an antenna array board. Copper (Cu) pillars act as low-loss interconnects between the RDL and the antenna substrate. To enable efficient signal transfer and minimize insertion loss, the semi-additive process is optimized to fabricate RDLs directly on embedded chips within an epoxy molding compound (EMC).**

The performance of these high-speed interconnects is evaluated through both simulation and S-parameter measurements. The signal path in the design includes grounded coplanar waveguides (GCPW) on the chips, coplanar waveguides (CPW) connecting the two chips, and their associated interfaces. The de-embedded insertion loss of the CWP connecting the 6 mm edge-to-edge chips at 180 GHz is approximately 10 dB, corresponding to a normalized loss below 1.9 dB/mm. This result aligns well with simulations and is comparable to state-of-the-art technologies.

Overall, this embedding-first approach effectively minimizes parasitic effects in chip-to-chip and chip-to-antenna connections. The techniques presented here could support the development of high-density, multi-layer RDLs with fine pitch and low parasitic loss, tailored for millimeter-wave (mmWave) applications.

***Index Terms*—chip embedding, semi-additive RDL, fan-out wafer-level packaging (FOWLP), co-planar waveguide (CPW)**

I. INTRODUCTION

The rapid advancement of millimeter-wave (mmWave) wireless communication systems, particularly in applications such as 5G/6G, automotive radar, and high-speed data links, has driven the demand for highly integrated, high-performance

packaging solutions. Recent improvements in the design of RF components in the sub-THz (sub-THz) frequency range have opened new possibilities for short-distance wireless communication within electronic systems [1]. However, meeting the performance requirements of mmWave components at these frequencies necessitates the development of advanced packaging technologies. One of the key challenges in such systems is the efficient integration of embedded chips with antenna arrays while minimizing signal loss, power dissipation, and parasitic effects at frequencies exceeding 100 GHz [2], [3]. Traditional packaging methods often fall short in maintaining signal integrity at these high frequencies due to impedance mismatches, substrate losses, and parasitic inductance associated with interconnects. To address the limitations of wire bond inductance, embedded chip packaging techniques place devices within substrate cavities or multilayer structures [4]. This approach enables a planar surface for customized planar interconnects with controlled impedance, thereby improving high-frequency signal transmission.

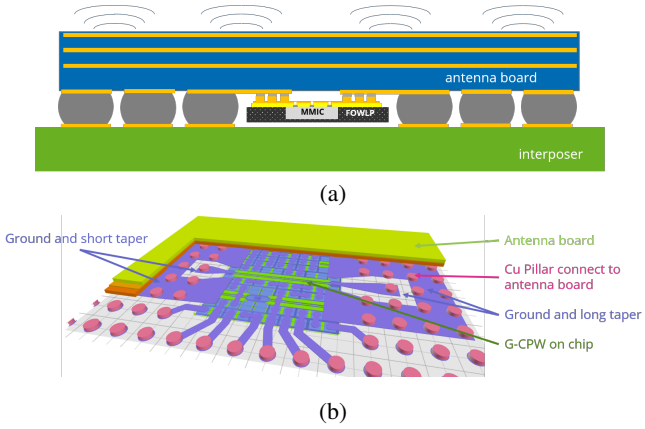


Fig. 1: The structure of the proposed fan-out wafer-level packaging (FOWLP): (a) FOWLP with embedded MMIC with RDL rewiring and 2nd level connection to the antenna board, and (b) The 3D illustration of the first level interconnection layers from chip-to-antenna.

In this paper, we examine an advanced packaging technology designed to integrate embedded chips with antennas for short-range mmWave communication at 180 GHz. We propose a fan-out wafer-level packaging (FOWLP) approach [5] utilizing a semi-additive redistribution layer (RDL) to route high-frequency signals from the embedded die to an antenna array board. Copper (Cu) pillars serve as low-loss interconnects between the RDL and the antenna substrate, ensuring efficient signal transfer and minimal insertion loss, as shown in Fig. 1 (a). This procedure allows a mmWave IC (MMIC) to be connected to a suitable antenna [6]–[8].

A key focus of this work is the design and fabrication of semi-additive RDLs incorporating optimized coplanar waveguide (CPW) structures to support high-frequency signal transmission within a compact footprint. To enable high-density, fine-pitch interconnects while minimizing parasitic effects, we develop a tailored manufacturing process by investigating various CPW geometries and evaluating their behavior at high frequencies. Furthermore, the signal integrity of chip-to-chip and chip-to-antenna connections is characterized to validate the performance of the proposed integration scheme.

The objective of this study is to advance mmWave packaging technology by developing low-loss, high-frequency interconnects across heterogeneous substrates. This approach supports the design of compact, highly integrated mmWave Antenna-in-Package (AiP) modules for emerging short-range wireless communication applications.

II. TECHNOLOGY ADVANCEMENTS

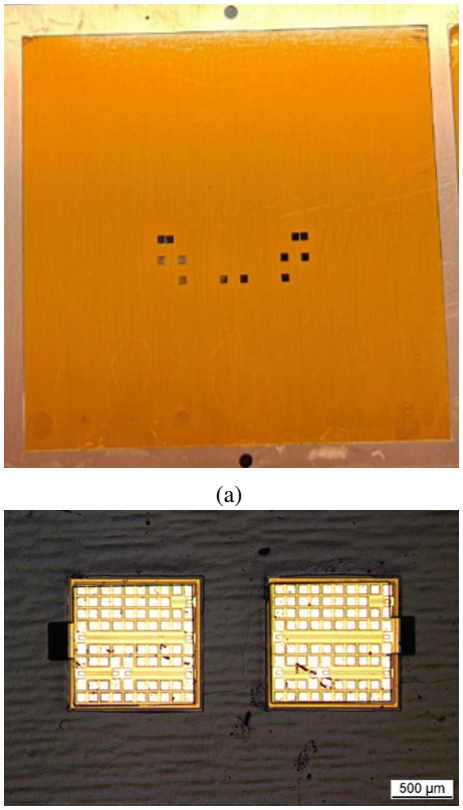
A. Test Chip and Array Embedding

As a proof of concept, test chips featuring multiple grounded coplanar waveguide (GCPW) transmission lines were designed and fabricated to evaluate RF performance. The embedding-first technology, previously developed and evaluated for application-specific, lab-scale processes [9], serves as the foundation for this work. In this approach, dies are initially embedded in an epoxy mold compound (EMC), enabling the subsequent formation of semi-additive redistribution layers (RDLs) with well-defined interconnect distances. EMC is a widely used encapsulation material in semiconductor packaging due to its favorable properties, such as good fluidity when heated, compatibility with molding complex structures, low thermal conductivity, and strong corrosion resistance. While EMC supports mechanical and chemical stability, its transmission loss at high frequencies must be carefully characterized to ensure suitability for mmWave applications.

In this work, the RF performance of the first-level interconnect, which is the RDL directly on top of EMC, is investigated. The chip-to-chip connection has been built using an RDL structured as a CPW. This configuration allows direct measurement of the signal transmission through the pair of embedded chips and the CPW interconnect, enabling de-embedding of the CPW transmission loss from the overall measurement. To accommodate RDL interconnects of varying lengths, the chips were precisely placed on an adhesive carrier with three different edge-to-edge spacings: 1.1 mm, 3 mm, and 6 mm, as illustrated in Fig. 2a. After placement, the chips were embedded in epoxy molding compound (EMC) and released from the temporary carrier. This step ensured mechanical stability while enabling subsequent RDL fabrication. The microscope image of a pair of embedded chips with the shortest reference connection of 1.1 mm and with a dielectric structure covering layer is shown in Fig. 2b.

B. Semi-Additive Redistribution Layer Fabrication with Optimized Coplanar Waveguide Design

The RDL fabrication process began with the deposition of a photo-definable dielectric layer using a PPE-copolymer (KMSF), selected for its low dielectric constant (Dk = 2.5) and low dissipation factor (Df = 0.003), both of which are critical for maintaining signal integrity at mmWave frequencies. The dielectric was spin-coated at a rotational speed of 2000 rpm to achieve a final thickness of 4 µm. It was then patterned



(a)

(b)

Fig. 2: The processes of chip embedding in EMC: (a) the chip array placed on adhesive tape for embedding, (b) A pair of embedded chips.

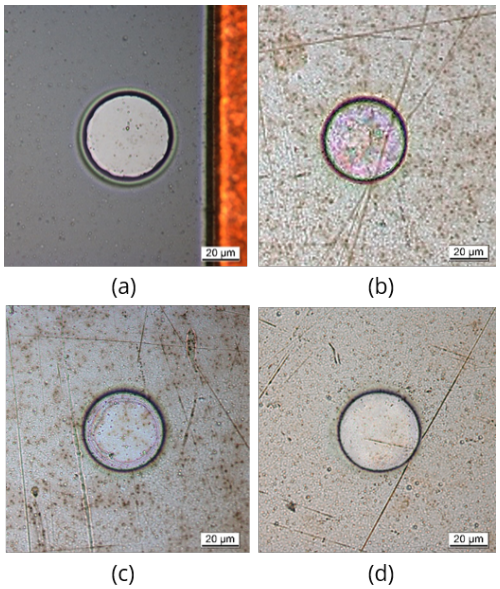
via direct writing laser lithography to open windows for conductive interconnects on the chip pads. Then, after the curing process, it was followed by a metallization process of:

- Step 1 - Sputtering: A 50-nm tungsten-titanium (WTi) barrier layer and 500-nm Cu seed layer were deposited. Before sputtering, a 20-minute 100W ion beam etching step was performed to remove the native oxide layer on the aluminum pads, ensuring good adhesion and electrical contact.
- Step 2 - Temporary resist layer formation: A photoresist layer was spin-coated and patterned via lithography to define the geometry of the CPW traces. These patterns guided the subsequent electroplating process.
- Step 3 -Electroplating: Copper was electroplated into the defined openings to form the CPW structures. The final thickness of the plated copper, 4 µm, was controlled by the electroplating time. Afterward, the temporary resist was stripped away.
- Step 4 - Seed layer etching: The unwanted Cu seed layer and WTi barrier layer were etched away, leaving behind the final CPW structures that electrically connect the embedded chip pair at the defined spacing.

After completing the fabrication processes, a semi-additive RDL interconnect was formed between each pair of embedded

Fig. 3: The CPW structure connecting 6 pairs of chips with 3 different distances.

chips, as shown in Fig. 3. To investigate the impact of taper geometry on signal integrity, two different CPW designs were implemented: a short-taper CPW, which minimizes the transition length, and a long-taper CPW, which provides improved impedance matching. These CPW structures served as the interconnects between chips, with taper profiles specifically optimized to reduce impedance discontinuities. The layouts of the short- and long-taper designs are illustrated in Fig. 1(b).



(a) (b)

(c) (d)

Fig. 4: Opening of the dielectric layer with different plasma treatment: (a) Si surface with 3 min plasma treatment. (b) Al surface with 3 min plasma treatment. (c) Al surface with 6 min plasma treatment. (d) Al surface with 9 min plasma treatment.

The study revealed significant variability in the DC resistance measurements of the daisy-chain structures on the test chip, depending on the sample. The high-frequency (HF) pads measuring (30 × 50) µm^2 are substantially smaller than the DC pads (80 × 80) µm^{2}and were more prone to open circuits or exhibited significantly increased resistance. In contrast, the larger DC pads consistently remained conductive. These observations suggest that residual contamination rather than surface oxidation is the primary cause of poor electrical contact.

Additionally, the aluminum (Al) surface exhibited different performance from the silicon (Si) surface in the dielectric material lithography process. As shown in Fig. 4, a further test was conducted to examine the influence on the dielectric

opening. The results showed that the transparent dielectric material showed a ring of light rainbow coloration at the structured opening. It was noticeably smaller on the Al surface and featured, indicating the presence of a thin residual dielectric layer. However, a 9-minute plasma treatment was sufficient to fully remove this unexposed residue, to prevent potential reliability concerns in high-frequency applications.

III. DESIGN AND SIMULATION

A. Signal Path Considering Antenna Design and Simulation

As introduced in [7], an AiP featuring a high-gain 8×8 patch antenna array operating at $180\,\mathrm{GHz}$ was designed to support short-range chip-to-chip or board-to-board communication. The antenna is implemented on a multilayer MCF-400HS laminate, utilizing aperture coupling to excite the stacked patch structure. The system supports up to four independent communication links, with beam steering achieved through integrated delay lines. The multilayer material stack is shown in Fig. 5, and the beam-steered wireless communication scenario is depicted in Fig. 6.

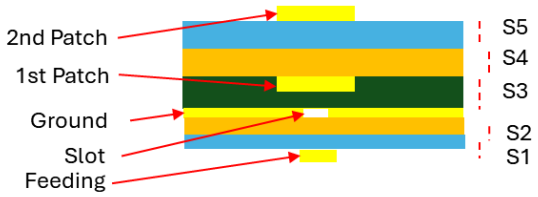


Fig. 5: Material stack-up of the AiP antenna using multilayer substrate with integrated aperture-coupled stacked patches [7].

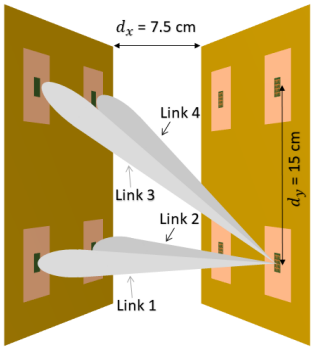


Fig. 6: Wireless board-to-board communication scenario for four links [7].

To evaluate vertical signal transmission through a realistic interconnect and packaging stack, a test structure was simulated that includes all key interface elements. The signal path begins at a GSG-compatible pad, transitions through a Cu pillar to an embedded interconnect, and enters a $1\,\mathrm{mm}$ GCPW line within the RDL. On the opposite side, the configuration is mirrored to reach another GSG pad. This structure emulates a realistic connection path for chip-to-chip or chip-to-antenna integration. The local interconnect geometry is shown in Fig. 7, and the complete cross-layer structure is illustrated in Fig. 8.

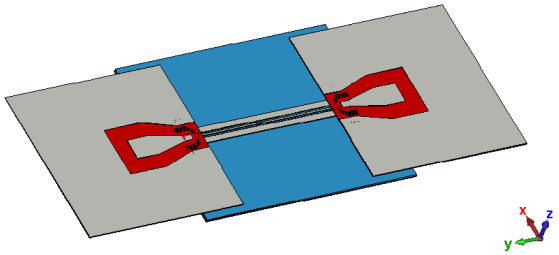


Fig. 7: 3D model showing the interconnects on either side of the

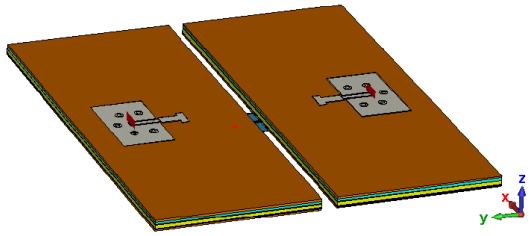


Fig. 8: 3D model showing complete signal path from GSG pad through Cu pillar, interconnect, and RDL to the opposite side.

The top-side GSG pad design follows the dual-aperture coupling concept introduced in [10], enabling on-wafer measurement without vertical vias or bond wires.

The simulated transmission coefficient S_{21} for the entire signal path is presented in Fig. 9. Across the frequency range from $160\,\mathrm{GHz}$ to $200\,\mathrm{GHz}$, the transmission loss varies from $-4.5\,\mathrm{dB}$ to $-11.1\,\mathrm{dB}$, with an average value of $-7.3\,\mathrm{dB}$. At the target frequency of $180\,\mathrm{GHz}$, a transmission of $-6.47\,\mathrm{dB}$ is achieved. Compared to the CPW-only results in Fig. 14, which exclude vertical transitions, this result confirms that the combined stack of pad, Cu pillar, interconnect, and RDL maintains acceptable performance for mmWave packaging.

B. Coplanar Waveguide Design and Simulation

The DC characterization for the proposed RDL structures is presented in previous work [11]. The technological improvement is carried out for Al HF pads with opening dimensions of $(30 \times 50)\ \mu\mathrm{m}^2$. Afterwards, the RDL's transmission loss was quantified by on-chip GCPW baseline measurement extracting S-parameters of the standalone GCPW lines on the test chips to establish a reference. In the subsequent chip-to-chip CPW characterisation S-parameters of interconnected chip pairs via RDL CPWs were measured across the three chip pitches. Finally, the de-embedding of RDL Loss was performed by comparing the two datasets. The insertion loss attributable solely to the RDL was isolated, enabling

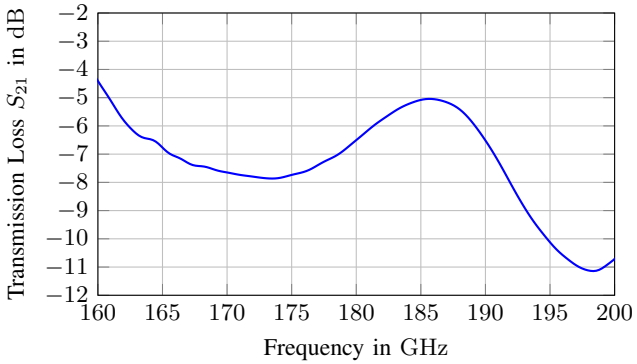


Fig. 9: Simulated transmission coefficient S_{21} from GSG pad through Cu pillar, interconnect, and 1 mm GCPW to opposite GSG pad.

evaluation of the CPW's high-frequency performance. This methodology allowed a systematic analysis of dielectric losses and interconnect parasitics at 180 GHz. By measuring the S-parameters of the GCPW lines on chip and comparing them to the measurement results from the pairs of chips that are connected by the CPW structure, the transmission loss of the RDL could be isolated.

For high-speed connections in the package from chip-to-chip and chip-to-antenna, we investigated different CPW structures. Given the 100 µm pitch of the embedded silicon chip pads, the interconnect structure must transition to a finer geometry to ensure proper connectivity. However, to minimize transmission losses, the main CPW section employs wider signal lines and spacing (100 µm). This necessitates a tapered transition between the chip pads and the CPW. Two distinct taper designs were implemented: a longer taper with 400 µm length has been designed to optimize the impedance matching to 50 Ω at a chip pitch of 3 mm, although it requires the space of two Cu pillars to connect to the antenna board; and a shorter taper with 200 µm length to minimizes transition length, to fit within the 200 µm pitch of the Cu pillar array, and to prioritizes compactness while maintaining signal integrity.

The resulting CPW structures feature slightly different center conductor widths (100 µm vs. 120 µm), as illustrated in Fig. 12 for 100 µm width and 6 mm length. The first taper structure has a longer length of 400 µm, and the latter has a shorter length of 200 µm. In Figure 1 (b), the different geometries of the tapers are displayed next to each other.

Taper length had a negligible impact on overall loss compared to the dominant influence of CPW trace length (see Figure 10). This suggests that miniaturizing the taper does not degrade performance, enabling a more compact interconnect design without sacrificing signal integrity.

This insight supports the use of shorter tapers in high-density packaging, where space constraints are critical, while maintaining low-loss transmission for 180 GHz applications.

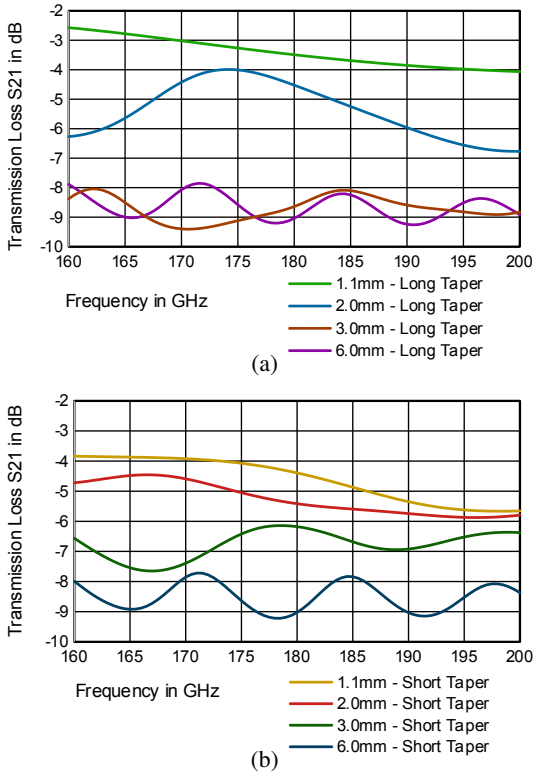


Fig. 10: Simulated transmission loss of co-planar waveguide with (a) a center conductor width of 100 µm and 400 µm long tapers and (b) a center conductor width of 120 µm and 200 µm long tapers at different chip distances.

IV. RF Characterization

A. De-embedding of the CPW Loss

To accurately assess the performance of the RDL interconnects, a reference measurement was first established by characterizing the intrinsic loss of the GCPW transmission lines fabricated directly on the test chips. These measurements were conducted using on-wafer probing with ground-signal-ground (GSG) probes, matched to the pitch of the chip pads. The S-parameters of the standalone on-chip GCPW lines were measured from DC to 200 GHz. Baseline insertion loss (IL) and return loss (RL) data from these measurements were used to de-embed the contribution of the chip's native GCPW lines from the overall system loss. Subsequently, the same GSG probes were used to measure the input/output of the chip-to-RDL-to-chip daisy chain structures. The same calibration technique (LRM or SOLT) was applied to ensure measurement consistency across both setups. The resulting S-parameters, also recorded from DC to 200 GHz, reflect the cumulative loss of the on-chip GCPW lines, RDL interconnects, and taper transitions, as illustrated in Fig. 11. Finally, the RDL's specific contribution to insertion loss was isolated by subtracting the baseline loss of the standalone chip from the total chip-to-chip measurement. This de-embedding step enables accurate quantification of the RDL interconnect performance, including taper-induced discontinuities and parasitic effects.

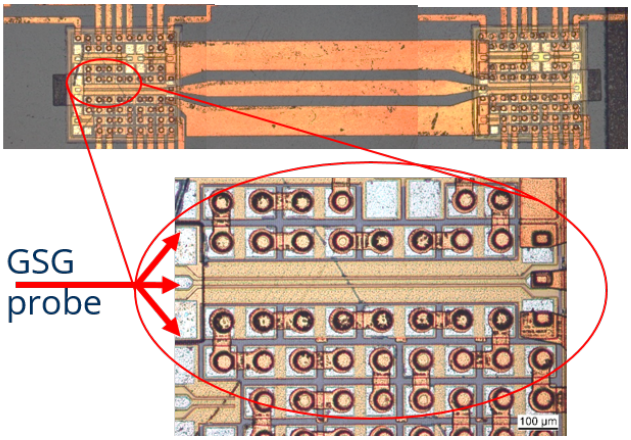


Fig. 11: The 6 mm CPW structure connecting a pair of chips. By measuring the S-parameter of the GSG structure on both sides of the chips, to determine the transmission loss

Figure 10 shows the simulated transmission loss in the targeted frequency range around 180 GHz for these two CPWs, including a taper on each end, and for the different chip-to-chip, or chip-to-antenna, pitches of 1.1 mm, 2.0 mm, 3.0 mm, and 6.0 mm. The comparison of the two different CPW structures at the same chip spacing differs much more between various distances, compared to the taper geometry. It can be seen that there is a periodic behavior over distance, indicating the slight deviation of the structure from the 50 Ω characteristic impedance.

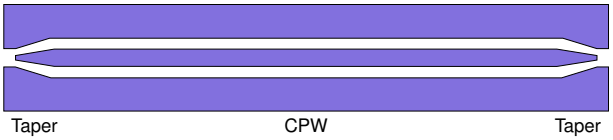


Fig. 12: Co-planar waveguide structure with center conductor width of 100 µm and a 400 µm long tapers for a test chip pitch of 6.0 mm.

B. S-parameter Measurements

The CPW structures were characterized on-wafer-prober with a Rohde & Schwarz ZVA-67 network analyzer and frequency converter modules. The setup was TRL-calibrated to the tips of the 100 µm GSG probes. To contact the CPW structures, a on-chip 50 Ω transmission line was used as an interface to the chip probes. The effect of this on-chip transmission line was de-embedded in post-processing, as described above. The measurement setup is shown in Fig. 13. Figure 14 compares simulations to two measurement results for the chip pitch of 6 mm. Transmission losses at 160 GHz are close to the predicted values from simulation; however, the losses have a steeper increase with frequency than predicted. The measured insertion loss of the signal path of 6 mm chip pitch, at 180 GHz is approximately 10 dB, considering the length of the CPW structure is corresponding to 5.2 µm, a normalized loss is 1.9 dB/mm Table I compares the loss per length of the presented CPW structure to typical values of different CPWs and packaging technologies. Regarding insertion loss, a performance similar to flip-chip has been shown.

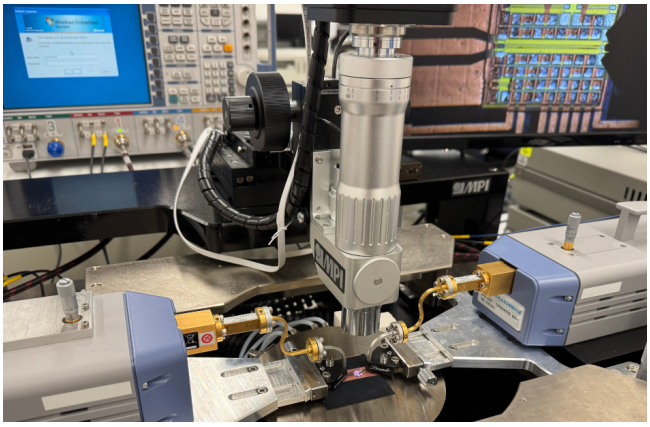


Fig. 13: S-Parameter measurement setup on-wafer-prober to characterize the high frequency behavior of the CPW structures.

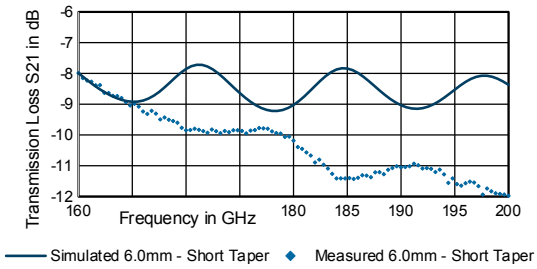


Fig. 14: Simulated and measured transmission loss of co-planar waveguide structure with a chip pitch of 6.0 mm.

V. CONCLUSION

This work experimentally investigates an advanced integration technology that connects embedded chips to antennas for high-frequency applications around 180 GHz. The primary objective was to minimize interconnect dimensions and electrical length to achieve low-loss connections by utilizing a semi-additive redistribution layer (RDL) for fan-out of the embedded chips. The main focus is to minimise the interconnect dimensions and electrical length to achieve a low-loss connection, using a semi-additive RDL for fan-out of the embedded chips. By evaluating semi-additive manufactured coplanar waveguide (CPW) structures designed for fine-pitch interconnects, a robust characterization method for the complete signal path was established. The measured insertion loss of the signal path of 6 mm edge-to-edge chips at 180 GHz is approximately 10 dB, corresponding to a normalized loss below 1.9 dB/mm, closely matching simulation results and comparable to state-of-the-art technologies. This validates the potential of the proposed fabrication and integration approach. The techniques demonstrated here can be extended to develop high-density, multi-layer RDLs with fine pitch and

TABLE I: Comparison of the insertion loss of different co-planar wave guide structures in different interconnect technologies.

	Center Width in µm	f in GHz	Insertion Loss in dB/mm	All Transitions Included in Loss	Reference
RO4350B CPW	100	70	0,1		[12]
		180	0,3		Extrapolated from [12]
PI foil CPW	10	180	0.6	X	[13]
Chip-to-Chip Bondwire Interface	17	180	9,2	X	[14]
Flip-Chip Interconnect CPW	10	180	1,9	X	[15]
eWLB CPW	90	70 - 110	0,3 - 0,4		[16]
		180	0,7		Extrapolated from [16]
On-Chip Aluminium GCPW	10	60	0,6		[8]
		180	1,5		Extrapolated from [8]
On-Chip Cu GCPW	10 - 5	180	0,5 - 1,0		Typical Values
This Work CPW – Short Taper	100	180	$< 1{,}9$	X	This Work

reduced parasitic effects, specifically tailored for mmWave systems. Different CPW geometries were investigated to optimize power transfer efficiency and minimize signal loss in a compact footprint.

For future work, addressing challenges related to metal layer roughness, which is an important factor in conductor losses, and improving embedding precision for even higher-frequency operation will be critical. The method presented here also enables systematic benchmarking of RDL-based interconnects against other technologies. While flip-chip integration currently offers the highest bandwidth potential, emerging hetero-integration approaches that combine multiple semiconductor technologies in a single package show promise for achieving comparable or superior performance in intra-chip connections.

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REFERENCES

[1] K. Nieweglowski, P. Seiler, D. Fritsche, S. Lüngen, D. Plettemeier, C. Carta, F. Ellinger, and K. Bock, "Interconnect technology development for 180ghz wireless mm-wave system-in-foil transceivers," in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, 2018, pp. 527–532.

[2] X. Gu, D. Liu, and B. Sadhu, "Packaging and antenna integration for silicon-based millimeter-wave phased arrays: 5g and beyond," *IEEE Journal of Microwaves*, vol. 1, no. 1, pp. 123–134, 2021.

[3] C. Hoyer, L. Steinweg, Z. Cao, V. Rieß, L. Li, F. Protze, C. Carta, J. Wagner, M. Kaynak, B. Tillack, and F. Ellinger, "Bendable 190-GHz Transmitter on 20-um Ultra-Thin SiGe BiCMOS," *IEEE Journal on Flexible Electronics*, vol. 1, no. 2, pp. 122–133, 2022.

[4] W. Heinrich, M. Hossain, S. Sinha, F.-J. Schmückle, R. Doerner, V. Krozer, and N. Weimann, "Connecting chips with more than 100 ghz bandwidth," *IEEE Journal of Microwaves*, vol. 1, no. 1, pp. 364–373, 2021.

[5] M. Chernobryvko, M. P. Kaiser, K. S. Murugesan, D. Kuylenstierna, J.-M. Köszegi, R. Gernhardt, T. Braun, I. Ndip, and M. Schneider-Ramelow, "High-q ku-band microstrip spiral resonator in fan-out wafer-level packaging (fowlp) technology for vco applications," in *2023 24th European Microelectronics and Packaging Conference & Exhibition (EMPC)*, 2023, pp. 1–4.

[6] C. Hoyer, L. Steinweg, F. Protze, F. A. Dürrwald, T. Meister, and F. Ellinger, "230 GHz Signal Generator for High-Bandwidth Data Links in 130 nm SiGe BiCMOS," in *2024 IEEE 24th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*. IEEE, Jan. 2024.

[7] M. Sohrabi, R. Yin, B. Klein, K. Nieweglowski, K. Bock, and D. Plettemeier, "Design of an antenna-in-package for 180 ghz chip-to-chip communication," in *2025 16th German Microwave Conference (GeMiC)*, 2025, pp. 25–28.

[8] R. Yin, H. P. E. Morath, C. Hoyer, K. Nieweglowski, K. Meier, J. Wagner, F. Ellinger, and K. Bock, "Characterization of Embedded and Thinned RF Chips," in *2023 24th European Microelectronics and Packaging Conference & Exhibition (EMPC)*. IEEE, Sep. 2023.

[9] K. M. R. Yin, K. Nieweglowski and K. Bock, "Characterization of material adhesion in redistribution multilayer for embedded high-frequency packages," in *2022 IEEE 9th Electronics System-Integration Technology Conference (ESTC)*. IEEE, sep 2022, pp. 321–325.

[10] M. Sohrabi, B. Klein, and D. Plettemeier, "Dual aperture coupling: A novel feeding method for 180 ghz antenna array," in *2025 16th German Microwave Conference (GeMiC)*, 2025, pp. 258–261.

[11] R. Yin, K. Nieweglowski, K. Meier, and K. Bock, "Embedding of thinned rf chips and electrical redistribution layer characterization," in *2022 IEEE 24th Electronics Packaging Technology Conference (EPTC)*, 2022, pp. 52–56.

[12] R. Corporation, "RO4000 Laminates RO4003C and RO4350B - Data Sheet," 2022, online available: https://www.rogerscorp.com.

[13] K. Nieweglowski, P. Seiler, D. Fritsche, S. Lüngen, D. Plettemeier, C. Carta, F. Ellinger, and K. Bock, "Interconnect technology development for 180ghz wireless mm-wave system-in-foil transceivers," in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, 2018, pp. 527–532.

[14] F. A. Dürrwald, F. Protze, D. Cvetkovski, T. Meister, R. Kraemer, and F. Ellinger, "Low-loss GSG bondwire chip-to-chip interconnects from dc to 330 GHz," in *14th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, Jun. 2025.

[15] S. Monayakul, S. Sinha, C.-T. Wang, N. Weimann, F. J. Schmückle, M. Hrobak, V. Krozer, W. John, L. Weixelbaum, P. Wolter, O. Krüger, and W. Heinrich, "Flip-chip interconnects for 250 GHz modules," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 6, pp. 358–360, 2015.

[16] M. Wojnowski, R. Lachner, J. Böck, C. Wagner, F. Starzer, G. Sommer, K. Pressel, and R. Weigel, "Embedded wafer level ball grid array (eWLB) technology for millimeter-wave applications," in *2011 IEEE 13th Electronics Packaging Technology Conference*, 2011, pp. 423–429.