Low-Loss GSG Bondwire Chip-to-Chip Interconnects from DC to 330 GHz

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***Abstract*—This research work provides a measurement-backed analysis of a single-ended chip-to-chip bondwire interface (BWI) with a signal pattern of ground-signal-ground (GSG) designed for minimum insertion loss. Different approaches to reducing the bondwire length and signal disturbing factors at the intersection of two microchips (such as the scribe lines and sealrings) are investigated and compared. Reproducible, seamless measurements from DC to 330 GHz have successfully demonstrated that GSG bondwire interconnects with only 3 dB insertion loss at 300 GHz can be realized without the need for tailored on-chip structures, which are typically area-intensive and can significantly limit the bandwidth and universal applicability of the chip.**

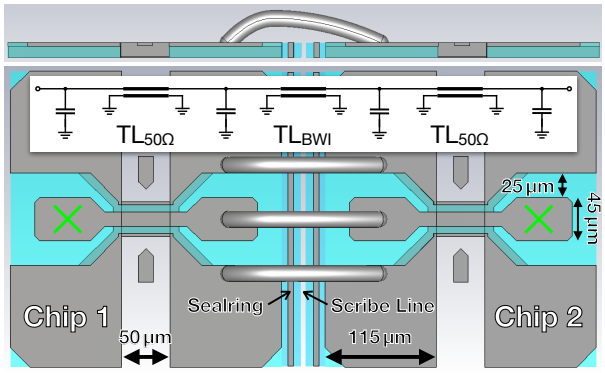
***Index Terms*—chip-to-chip interconnects, GSG interface, bondwire, millimeter wave, sub-THz, ultra-broadband packaging**

I. Introduction and State-of-the-Art

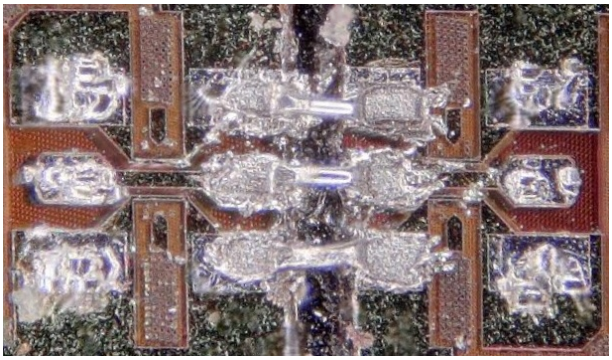
The optimization of electronic microsystems based on integrated circuits (ICs) typically involves a multi-stage process of designing and analyzing individual structures (e.g. amplifiers, mixers) before assembling them into larger systems (e.g. an integrated receiver frontend). Even with advanced software tools for functional evaluation readily available, it is usually necessary to characterize subsystems by on-wafer measurements with 50 Ω probes. However, especially at frequencies approaching the sub-THz range, this increasingly contradicts subsequent system integration via chip-to-chip interconnects, where losses dominate and tailored chip design is required.

A well-established technique for contacting microchip pads is wire bonding. Bondwires can be put into proximity of each other to resemble transmission line (TL) structures. For single-ended high-frequency interfaces, a GSG arrangement is used.

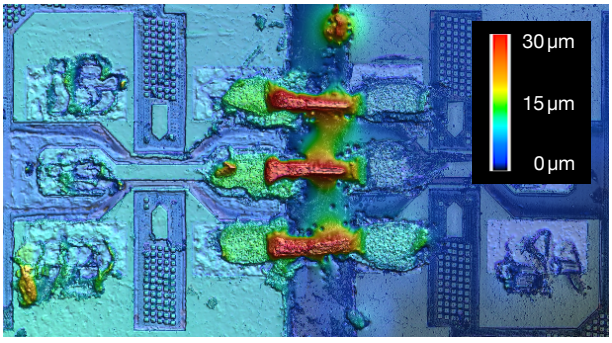
This principle is investigated up to 170 GHz in [1], where 1 dB insertion loss at 140 GHz is reported for interconnects enhanced by series reactive L-C-L networks and microstrip stubs, and 5 dB without any compensation. Differential GSSG bondwire interconnects at an even higher frequency range of 200 - 330 GHz are examined in [2], where measurements enabled by Marchand Baluns are presented, achieving around 6 dB loss at 330 GHz. The GSG bondwire transmission line section can be made $\lambda/2$ long for self-compensation, as shown in [3], achieving a narrow-band insertion loss of better than 2 dB at 60 GHz. In [4], such a large $\lambda/2$ structure is enhanced by adding dielectric encapsulation, presenting an optimum of better than 4 dB across 110 - 170 GHz with a minimum of 2 dB at 140 GHz. An alternative approach of magnetically coupling



(a) *CST* model and equivalent circuit. Cross-section (top) and top view (bottom) are to scale. The scribe line will be wider if not ground away.



(b) Perspective Microscope (*Keyence VHX-7000*): Micrograph.



(c) Laser Confocal Microscope (*Keyence VK-X3000*): Surface depth map. Note the slight difference in chip surface height due to gluing inaccuracy.

Fig. 1: Visual description of the proposed bondwire-based GSG chip-to-chip interface. General concept presented in (a) and special microscopy of a realized sample with ground away chip edge structures in (b) and (c).

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horizontal half-loop bondwires at 180 - 220 GHz is reported in [5], comparing the insertion loss of around 4 dB at 200 GHz to 18 dB of a conventional 350 µm long GSG interface. However, the latest advancements regarding such single-ended GSG arrangements, presented in [6], yield as low as 1 dB insertion loss at 210 GHz by elaborate tailoring to the system impedance introducing novel adhesive films and aluminum sheet encapsulations as well as 3D-printed microstructures for more precise alignment of the gold bondwires used. This is comparable even with the less flexible but high-performance alternative of flip-chip techniques as in [7].

The research work at hand also pursues the strategy of trying to match the system impedance, reducing insertion loss by further shortening the interface making use of chip edge grinding. Structures tailoring the IC to the interconnect properties such as matching and (self-)compensation approaches are avoided to allow for more universal chip application while also significantly increasing bandwidth and compactness.

Repeatable, seamless measurements are provided from DC to 330 GHz. The effect of the actual interface is extracted. The influence of chip edge structures such as the scribe lines and the sealrings as well as encapsulation are investigated.

II. Concept and Physical Realization

Bondwires are inductive in behaviour and can be modelled as corresponding lumped elements. In combination with pad capacitances, higher-order low-pass filters are formed, significantly limiting usable bandwidth of such interconnects. However, when placing other conductive elements tied to ground nearby (such as two lateral ground bondwires), introducing capacitance to the cross-section, a transmission line structure is formed, whose properties can be controlled as follows:

- Placing the conductors as close together as practical for the particular bonding process to increase capacitive coupling and thus reduce characteristic line impedance, ideally matching the system impedance of $50\,\Omega$. For a GSG center-to-center bondwire distance of $55\mu\mathrm{m}$ and an SiO_2 volume (chip substrate) below ($\varepsilon_{\mathrm{r,eff}} = 1.92$), a clean quasi-TEM excitation via a multipin waveguide port setup in *CST* extracts a line impedance of $105\,\Omega$. An optimum of about $50\,\Omega$ would be reached for a spacing of $24\,\mu\mathrm{m}$, which is too narrow for the available bonding process.
- However, a dielectric encapsulation can reduce the characteristic line impedance for a given spacing. For example, a hypothetical full encapsulation in SiO_2 ($\varepsilon_{\mathrm{r}} = 4.1$) of the GSG conductors spaced at $55\mu\mathrm{m}$ would yield $72\,\Omega$.
- Shortening the bondwires to reduce inherent transmission line losses. This is particularly important if a sufficient transmission line arrangement cannot be formed and a mismatch to the system impedance is present.
- Realizing the bondwire loops strictly parallel and flat, keeping the interface cross-section (with the electromagnetic quasi-TEM waves encountering varying proportions of air and SiO_2) and characteristic impedance uniform.
- Using good conductors to minimize resistive losses and creating reliable bondwire attachments with the pads.

A. On-Chip Structures and IC Design Process

Fig. 1 shows the on-chip setup of two back-to-back general purpose low-capacitance GSG pads (suitable for probe pitches of 50 -100 µm as well as wire bonding) and a $50\,\mu\mathrm{m}$ long grounded coplanar waveguide (GCPW) transmission line of $50\,\Omega$ characteristic impedance inbetween. This line is added to ensure that the probe distance is always larger than in the calibration short- or thru-standards, avoiding direct signal crosstalk between the probes that isn't accounted for. Extra spacing between the probes and the bondwire interface is also beneficial for safely adding encapsulation to a sample.

IHP SG13G2Cu [8] was used as IC technology, which offers a high-frequency backend-of-line, where the topmost thick aluminum layer is assigned for GCPW signal conductors with about 13 µm of SiO_2 ($\varepsilon_{\mathrm{r}} = 4.1$) dielectric below. For creating the shortest possible bondwire connections from chip to chip, structural limitations at the chip edges are of interest, as shown to scale in Fig. 1a. Following a pad, placed as close the chip edge as possible as dictated by process design rules, a sealring (SR) provides electrical and mechanical protection for the active area. Following outwards, the scribe line (of about 55 µm width) prevents damage to the individual dies during wafer dicing. The sealring provides an additonal barrier against cracks that could form due to lateral stress from dicing and is therefore also sometimes referred to as crackstop.

B. Chip Arrangement, Bonding and Grinding Technique

Two of these chips are mounted next to each other on a rigid carrier board as shown in Fig. 1b, carefully leveling their surfaces by applying some vertical pressure, and connected by variations of the proposed bondwire interface. A conventional ultrasonic wedge-wedge bonder with 17 µm aluminum bondwire is used to realize the interconnects. In creating a bond, the wedge must follow a certain curve so that the first bond point is not sheared off from the pad. This creates the characteristic shape of a bond wire, refer again to Fig. 1a. However, the according upwards movement after setting the first bonding point results in additional height and thus overall bondwire length. To reduce this, the bondwire is carefully pushed back into the wedge before moving it horizontally to the side and setting the second point on the other pad. This way, a very short and flat interconnect, as measured in Fig. 1c, is realized.

To remove the chip edge structures (scribe line and sealring), a grinding arrangement based on a rotating polishing disk is experimented with. This approach was previously described in [9]. Applying elastic silicone disks with high rotation speeds but little pressure at a slight horizontal angle to the chip edge proved to be effective for fast and precise grinding with little risk of damaging the chip.

C. Encapsulation

For dielectric encapsulation, *Henkel LOCTITE Stycast 2850FT* epoxy resin with a high relative permittivity of $\varepsilon_{\mathrm{r}} = 6.45$ (defined at 1 MHz, as per datasheet) was chosen. Its viscosity is controlled by adjusting the mixing ratio with catalyst *LOCTITE CAT 24LV* to tighly cover the bondwires

without flooding the adjacent chip pads used for probing. The resulting glob top cures at room temperature. The high-permittivity dielectric provides mechanical stability and environmental protection to the structure, while reducing the characteristic impedance for a given line spacing as desired.

III. Measurement Setup

A. General Equipment

Two-port S-parameter measurements were performed in a laboratory using a manual wafer prober station and a *Rohde & Schwarz ZVA67* vector network analyzer (VNA), see Fig. 2. To seamlessly cover the very wide frequency range up to 330 GHz, different converter module extensions as listed in Tab. I were used. All samples were probed in calibrated setups.

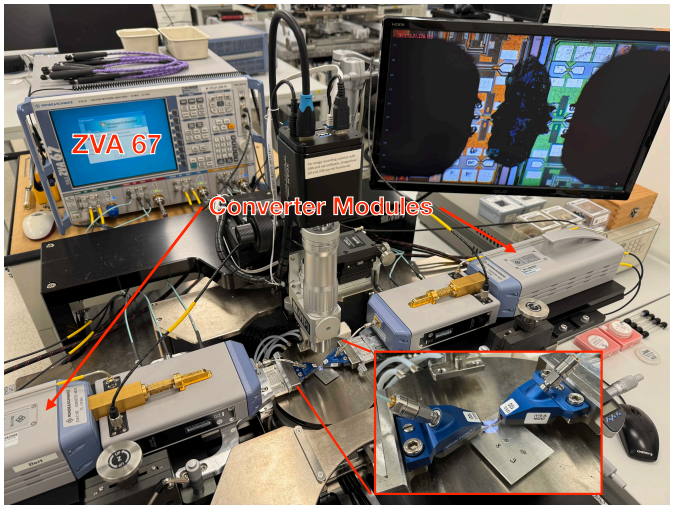

Fig. 2: Measurement setup based on wafer probing and converter modules for frequency range extension of the VNA. Previous VNA power calibration with the *Rohde & Schwarz ZVA67* thermal power sensor NRP110T is advisable. An encapsulated sample without chip edge grinding was measured here.

B. Calibration, De-embedding and Repeatability

Especially at triple-digit gigahertz frequencies, exact probe placement on the pads is essential for accurate and repeatable measurements, so a strict center position on the pads as marked in Fig. 1a was ensured at all times. The warmed-up measurement setup was calibrated to the probe tips using the impedance standard substrates in Tab. I and the calibration methods LRM+ (checked with SOLT) up to 140 GHz and TRL above. The reference plane is shifted to the center of the pads.

Precise measurements rely on the exact probe overtravel values (identical to calibration) in Tab. I and clean electrical contacts. This is why mechanical wear of the soft aluminum pads, see Fig. 1b, is problematic. So measurements were taken starting with the highest frequencies, which require smaller overtravel values. Some variations from sample to sample are to be expected resulting from manual grinding and bonding.

The on-chip feeding networks $\mathrm{TL}_{50\,\Omega}$ at the input and output, ref. to Fig. 1a, although designed to feed the signals to the bondwire interface in a neutral manner (matching the system impedance of $50\,\Omega$) were then de-embedded from the measurement data of a combined sample to account for inherent losses at the upper end of the overall frequency range.

TABLE I: S-parameter probing equipment for all frequency ranges.

Frequency Range	Converter Module	Probe Type	Calibration Substrate	Probe Overtravel
0 - 67 GHz*	-	Cascade Infinity i67-A-GSG-100	Cascade 101-190	50 µm
75 - 110 GHz*	R&S ZVA-Z110E	Cascade Infinity i110-A-GSG-100	Cascade 138-375	30 µm
90 - 140 GHz (WR8)	R&S ZVA-Z140	Cascade Infinity i140-GSG-100-BT	Cascade 138-357	30 µm
140 - 220 GHz (WR5)	R&S ZVA-Z220	GGB 220-GSG-100-BT	GGB CS-15	25 µm
220 - 330 GHz (WR3)	R&S ZC-330	GGB 325B-GSG-75-BT	GGB CS-15	15 µm

* Seamlessly interleaved by using a diplexer extension setup.

Scattering transfer parameters (T-parameters), defined as

$$\begin{aligned}\begin{pmatrix} b_1 \\ a_1 \end{pmatrix} &= \mathbf{T} \begin{pmatrix} a_2 \\ b_2 \end{pmatrix} = \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} \begin{pmatrix} a_2 \\ b_2 \end{pmatrix} \\ &= \begin{pmatrix} \frac{S_{12}S_{21}-S_{11}S_{22}}{S_{21}} & \frac{S_{11}}{S_{21}} \\ -\frac{S_{22}}{S_{21}} & \frac{1}{S_{21}} \end{pmatrix} \begin{pmatrix} a_2 \\ b_2 \end{pmatrix}, \end{aligned} \tag{1}$$

allow for cascading of 2-port networks by considering all bidirectional interactions of incident waves a and reflected waves b in an according chain. To extract the bondwire interface $\mathbf{T}_{\mathrm{BWI}}$ from the measurement data $\mathbf{T}_{\mathrm{meas}}$, equal port and reference impedances of $50\,\Omega$ provided, the wave effects of "test fixture" in- and output networks $\mathbf{T}_{\mathrm{TL}_{50\,\Omega}}$ are removed by

$$(\mathbf{T}_{\mathrm{BWI}}) = (\mathbf{T}_{\mathrm{TL}_{50\,\Omega}})^{-1}(\mathbf{T}_{\mathrm{meas}})(\mathbf{T}_{\mathrm{TL}_{50\,\Omega}})^{-1}\,. \tag{2}$$

S_{21} is then calculated from $\mathbf{T}_{\mathrm{BWI}}$ by $S_{21} = 1/T_{22}$. [10] (Inverse) T-parameter matrices are obtained from S-parameters.

IV. Measurement Results and Discussion

Overall, the measured bondwire interface samples with chip edge grinding reliably show an insertion loss S_{21} of better than 4.4 dB at 330 GHz, with the best one improving it to just 1.6 dB, refer to Fig. 3. The average -3 dB-bandwidth of S_{21} is about 300 GHz. After a plateau with minimum losses up to about 100 GHz, an attenuation increasing with a very shallow gradient is observed. This is beneficial for even more broadband and/or higher center frequency signal transmission applications (e.g. requiring good linearity and minimum group delay). Models of an effective (partially compensated) series inductance of 400 pH/mm acting as a first-order low-pass filter on the one hand and a $100\,\Omega$ transmission line on the other hand as well as 3D-FEM simulations in *CST* fit the observations. Removing the sealring consistently improves performance, pointing to less disruptive quasi-TEM wave progation with the substrate portion cleared of discontinuities. Compared to a sample without grinding, shown in Fig. 4, there are even greater gains across the entire frequency range. Dielectric encapsulation (applied to previously measured samples to directly assess the effect on wave propagation) can reduce loss at some frequencies and is particularly beneficial for longer lines (as for chips without grinding), but at the cost of reduced S_{21} curve flatness. Several superimposed phenomena play a role here, such as the difficulty to evenly enclose the fine bondwire structures and a frequency dependence of the dielectric's permittivity.

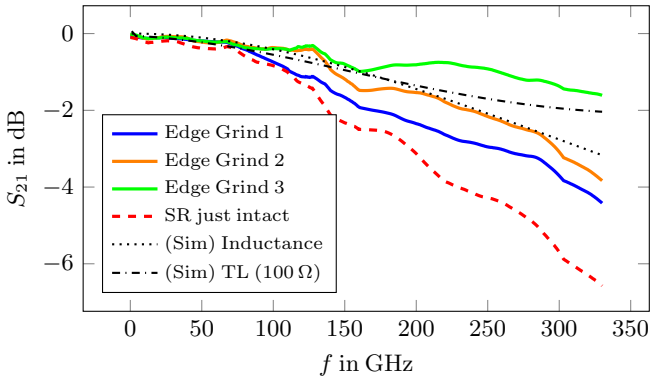

Fig. 3: Comparison of samples with chip edge grinding (removing scribe line and sealring). Sample Edge Grind 1 (134 µm pad center to pad center distance) is the one shown in Fig. 1. Sample 3 was a more aggressive grind (109 µm), not only removing the sealring but grinding up to the pad center conductor. For comparison, a sample where the scribe line was removed but the sealring is just intact (228 µm) is given. Exemplary simulation results for a 50 pH series inductor and a 100 Ω TL of 125µm length are compared.

$\lambda/2 = 363\,\mu\text{m}$ at 300 GHz for an estimated $\varepsilon_{\text{r,eff}} = 1.9$, so the presented guided wave structures are well below $\lambda/2$ or $\lambda/4$ and can be considered electrically short. Therefore, narrowband transmission line effects based on reflections, such as impedance transformation, are less pronounced. This results in a flat, low-loss transmission behavior and mitigates the effects of not being able to match the system impedance exactly due to bondwire manufacturing constraints.

Fig. 5 shows the input matching, which is very close to the center of the Smith chart for the chips with ground edge areas. Its magnitude stays below -8 dB. In terms of DC evaluation, all measured samples have a series resistance of 3.9 - 4.1 Ω.

The results are competitive even with the most advanced interconnects in the state-of-the art as in [6], without requiring the same amount of high-precision assembly effort.

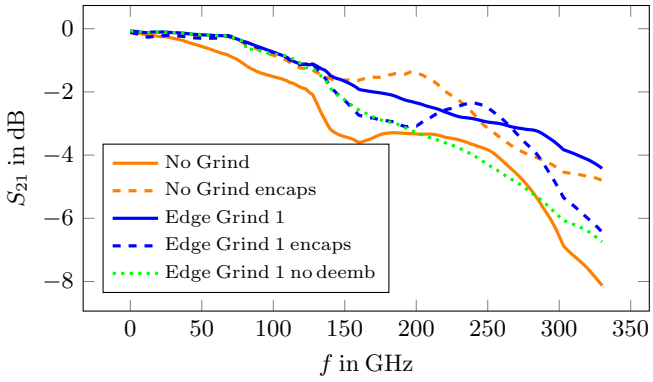

Fig. 4: Comparison of sample Edge Grind 1 from Fig. 3 (being the worst one in terms of insertion loss) to a sample without any edge grinding (No Grind). The respective results for encapsulation (encaps) are added. Exemplary raw data without T-parameter based de-embedding (no deemb) is also shown.

V. Conclusion

The presented GSG bondwire interface approach based on chip edge grinding reliably achieves a low insertion loss of less than 3 dB up to 300 GHz by realizing electrically short transmission lines close to the system impedance. This solution is inexpensive and versatile, because it is very broadband and does not require any additional on-chip matching

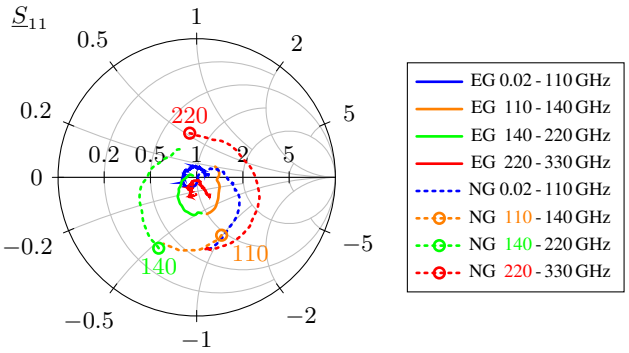

Fig. 5: Smith chart visualizing the input matching of sample Edge Grind 1 (EG) vs. a sample without grinding (NG) for a 50 Ω termination. The measurements for the different frequency ranges align well, small discontinuities at the higher frequency band edges are to be expected. As is some noise in the immidiate vicinity of a perfect match. Measurements were reciprocal.

structures, which simplifies modular system integration. Repeatable, seamless measurements from DC to 330 GHz give indications for possible applications of this universal approach.

Acknowledgment

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