Low Phase Noise 104 GHz Oscillator Using Self-Aligned On-Chip Voltage-Tunable Spherical Dielectric Resonator in 130-nm SiGe BiCMOS

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***Abstract*—This paper studies a low phase noise voltage-controlled oscillator that is based on a self-aligned on-chip voltage-tunable spherical dielectric resonator. The proposed resonator has been designed for millimeter-wave applications, provides a high quality factor and is voltage controlled. To prove the concept, the circuit is implemented in a 130-nm SiGe BiCMOS technology. It consists of a two stage amplifier and a microstrip feedback path which couples to the resonator. Measurement results demonstrate a phase noise of -95.9 dBc/Hz at 10 MHz offset from the oscillation frequency at 104.03 GHz and a frequency tuning range of 88 MHz. A maximum output power of -9.9 dBm from 32.5 mW dc power is achieved. Simulations based on measurements of the on-chip spherical dielectric resonator indicate that circuit optimizations will lead to an excellent phase noise of -114.8 dBc/Hz at 10 MHz offset. To the best of the authors' knowledge, this circuit is the first reported silicon-based MMIC voltage-controlled oscillator using an on-chip dielectric resonator at millimeter-wave band.**

***Index Terms*—SiGe, dielectric resonator, Q-factor, phase noise (PN), mm-wave oscillators**

I. Introduction

Millimeter-wave (mm-wave) and sub-terahertz (sub-THz) silicon-based integrated systems are becoming more attractive for applications like high data rate wireless communication, close-range radar and ultra-wideband imaging. As a result of the low quality factor (Q-factor) of integrated LC tanks, limited tuning range of the varactors, and increasing operating frequencies the required mm-wave oscillator sources with low phase noise (PN) and excellent frequency stability are increasingly difficult to obtain.

Due to significant improvement of PN performance, which is largely determined by using high quality factor (high-Q) resonators, well-known high-Q dielectric resonators have been used at high frequencies to overcome the above shortcomings of mm-wave VCOs [1]. A dielectric resonator usually has properties such as high-Q and excellent resonance frequency stability against temperature change, thus a dielectric resonator oscillator (DRO) offers good PN and high frequency stability performance compared to other lumped element LC tank based VCOs in mm-wave frequencies. In this work, a spherical dielectric resonator (SDR) is investigated and used as an on-chip high-Q resonator [2], [3] for mm-wave VCOs. The SDRs operating in higher-order mode are used to solve problems relate to substrate resistivity, mechanical alignment precision and chip-area consumption, and have been demonstrated for mm-wave applications in recent years.

II. Design and Implementation of Oscillator

A. Voltage-Tunable Spherical Dielectric Resonator (VTSDR)

The VTSDR comprises a spherical resonator and a metal patch with varactors underneath it for center frequency tuning. Low-loss alumina ceramic spheres with a relative permittivity of around 10.15 and a diameter of 1 mm are used as dielectric resonators. A measured loaded Q-factor of 143 at 103 GHz has been achieved for a same SDR structure in [3]. The sphere is accurately self-aligned on the chip by placing it into an octagonally-shaped shallow cavity inside the back-end-of-line (BEOL) dielectric layers of silicon-based semiconductor circuit, as can be seen in Fig. 1(a). Therefore, the self-alignment of the resonator is achieved by the sphere falling into the cavity and then settling there. To prevent radiation leakage from the resonator while maintaining a high Q-factor, the sphere is covered with a top metal plate that is parallel to the substrate.

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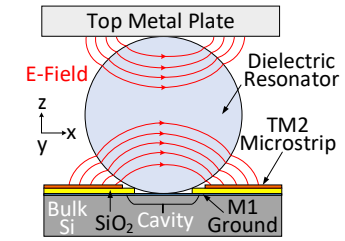
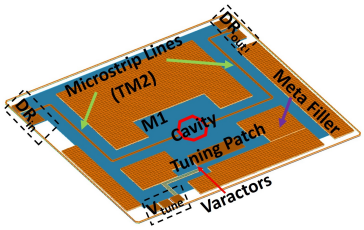


(a)



(b)

Fig. 1. VTSDR structure with the coupling microstrip lines: (a) cross-section of the on-chip VTSDR with a top metal plate, (b) 3D-layout view.

Fig. 1(a) illustrates a high-Q resonance mode of the VTSDR structure orthogonal to the parallel-plate mode.

Furthermore, the sphere is loosely coupled to two open-ended microstrip lines from both sides to offer a high Q-factor, thus the loss of such resonators can be higher than 18 dB above 100 GHz. The ground planes (M1) of the microstrip lines (TM2) prevent leakage into the high-loss silicon substrate. In order to obtain a frequency-tunable dielectric resonator, a rectangular tuning patch is placed in the middle of two microstrip lines but below them, and carefully coupled to the sphere, as shown in Fig. 1(b). The varactors under the tuning patch are used for the voltage-controlled frequency tuning. All simulations here were performed with the 3D EM-solver of CST Microwave Studio.

B. Design of Amplifier and Buffer

In order to fulfill the oscillator conditions and to achieve sufficient gain above 20 dB, a two stage cascode amplifier is proposed. On the basis of negative resistance theory, the two stage amplifier is configured in parallel feedback generating the negative resistance to over compensate the loss from the resonator. To retain the advantages of the high-Q resonator and its crucial impact on the PN of the oscillator, the active part of the circuit has to isolate it from the 50 Ω output load that could otherwise lower its Q-factor and thus decrease the PN. Therefore, a high-impedance output buffer is implemented to match the output of the oscillator for the high-Q resonator.

The circuit schematic of the designed amplifier and buffer is shown in Fig. 2. According to the post-layout simulations, this two stage amplifier achieves a peak gain of 27.4 dB at 103.4 GHz with a 3-dB bandwidth from 92.5 GHz to 111.5 GHz. The output buffer provides a simulated maximum output power of 5.5 dBm.

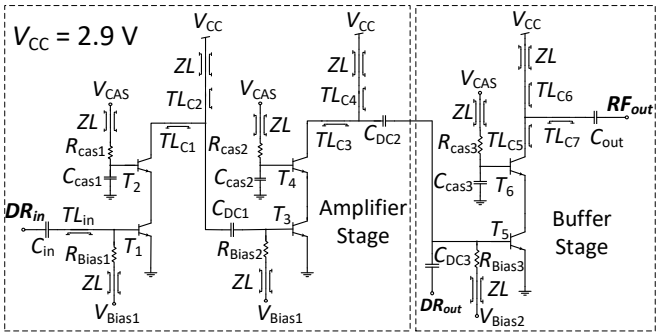
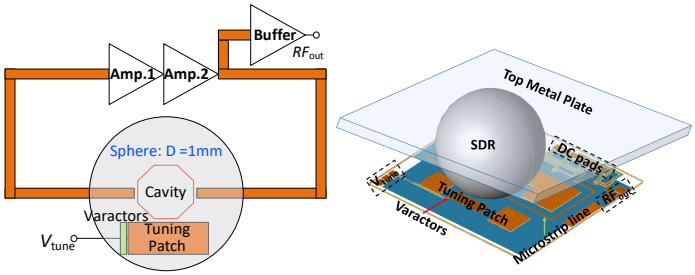


Fig. 2. Schematic of the designed amplifier and buffer.



(a) (b)

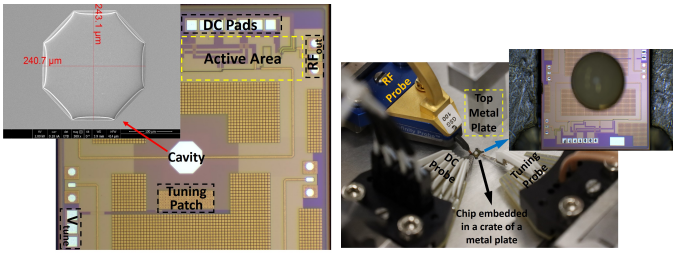
Fig. 3. The proposed VCDRO chip including the top metal plate: (a) block diagram, (b) 3D-layout view.

C. Design of Voltage-Controlled Dielectric Resonator Oscillator (VCDRO)

A corresponding circuit block diagram representing the proposed VCDRO is given in Fig. 3(a). It consists of a tunable resonator network in the parallel feedback loop, a two stage amplifier, and an output buffer. To realize the oscillation and fulfill the oscillation condition, the loop gain at the resonant frequency must be greater than one and the phase should equal zero. Two microstrip feed lines coupled to the on-chip SDR component serve not only as a physical connection, but also to adjust the phase between the resonator and the amplifier. The feedback gain is controlled by the coupling from the amplifier output to the amplifier input. Basically, the parallel feedback based dielectric resonator oscillator can be considered as a positive feedback amplifier with a VTSDR, which is used as a frequency-selective feedback element. An output buffer employed to isolate the resonator from the 50 Ω load is connected at the output of the oscillator to maintain the high-Q characteristics of the resonator. The frequency tuning is achieved by using the varactors connected to the tuning patch. Fig. 3(b) presents the complete 3D-layout view of the proposed VCDRO chip including the top metal plate. All co-simulations, which combine the circuit simulations and the EM model of VTSDR, were performed in Keysight ADS.

III. Experimental Results

To prove and investigate the concept, the circuit was fabricated in a 130-nm SiGe BiCMOS technology, which has a maximum f_T/f_{max} of 300 GHz/500 GHz. Fig. 4(a) shows the



(a) (b)

Fig. 4. (a) Micrograph of the fabricated VCDRO chip and FIB image of the on-chip cavity, (b) on-wafer measurement setup of the VCDRO chip.

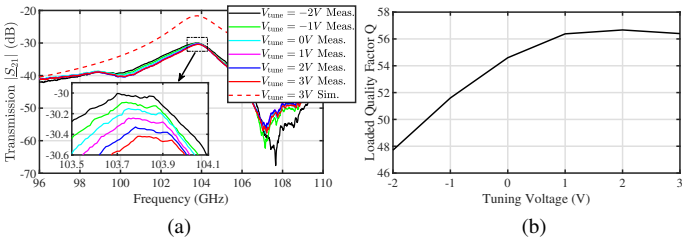
chip micrograph and the focused ion beam (FIB) micrograph of the on-chip cavity. The whole circuit occupies an area of 3.74 mm^2 containing all dc/rf pads. The total dc power is 32.5 mW, under a supply voltage of 2.9 V. The on-wafer measurement setup of the contacted chip is illustrated in Fig. 4(b). The chip is embedded into a crate of an aluminium plate and its surface is leveled with metal plate surface, to prevent electromagnetic leakage into the high-loss silicon substrate [3]. Due to mechanical limitations by the on-wafer probes, a small top metal plate with a width of 6 mm is directly placed above the sphere. Ideally this plate should be much larger. Moreover, it should be taken into account that the relative permittivity and the diameter of fabricated spheres vary slightly from sphere to sphere.

Fig. 5(a) presents the simulated and measured transmission coefficients at resonance frequencies of the VTSDR under different tuning voltage V_{tune} from -2 V to 3 V. The VTSDR demonstrates measured resonance frequencies between 103.7 GHz to 103.8 GHz with a forward transmission $|\underline{S}_{21}|$ of around -30.3 dB. The simulated resonance frequency under a tuning voltage of 3 V appears at 103.8 GHz with a forward transmission $|\underline{S}_{21}|$ of -21.6 dB. In order to realize a very high Q-factor, the dielectric resonator is usually loosely coupled to the open-ended microstrip lines for the on-chip resonator applications, thus the transmission loss is pretty high in some cases. A good compromise between loss and Q-factor has been investigated during the design. According to [3], all measured resonator transmission losses are higher than 30 dB at around 102 GHz. The reasons for the higher measured losses than the simulations are suspected to be caused by the radiation leakage out of two small parallel metal plates and excess loss in the thick bulk silicon through the chip edges. The measured loaded Q-factor (Q_{L}) of the VTSDR as a function of tuning voltage V_{tune} is shown in Fig. 5(b). Compared with the simulated highest loaded Q-factor of 52.9 with V_{tune} = 3 V, the measured highest loaded Q-factor of 56.7 with V_{tune} = 2 V is provided. The corresponding Q_{L} is defined as [4]:

$$Q_{\text{L}} = \frac{f_{\text{c}}}{BW_{\text{3dB}}} \tag{1}$$

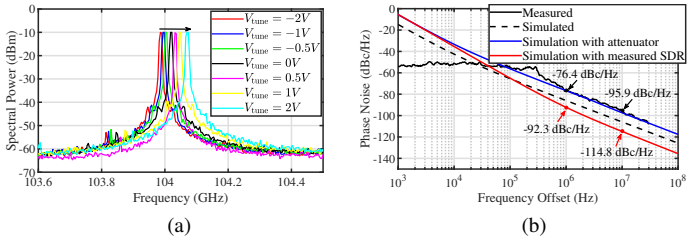
where f_{c} is the resonance frequency, and BW_{3dB} is the 3dB-bandwidth.

The measured output spectral power of the VCDRO with different tuning voltages V_{tune} is given in Fig. 6(a). Measurement results show a tuning range of 88 MHz from



(a) (b)

Fig. 5. (a) Simulated and measured $|\underline{S}_{21}|$ of the VTSDR under different V_{tune}, (b) measured loaded Q-factor of the VTSDR as a function of V_{tune}.



(a) (b)

Fig. 6. (a) Measured output spectral power of the VCDRO under different V_{tune}, (b) simulated and measured PN of the VCDRO.

103.986 GHz to 104.074 GHz by changing V_{tune} from -2 V to 2 V, and a maximum output power of -9.9 dBm. Moreover, original simulations show an expected PN of -85.9 dBc/Hz at 1 MHz offset and -106 dBc/Hz at 10 MHz offset from the oscillation frequency of 103.804 GHz in Fig. 6(b). However, measurements present a higher PN of -76.4 dBc/Hz at 1 MHz offset and -95.9 dBc/Hz at 10 MHz offset from the oscillation frequency of 104.03 GHz. We attribute this to a higher loss in the fabricated VTSDR, when compared to the losses predicted for the VTSDR by simulation. It leads to non-optimal loop gain and phase in the VCDRO circuit, and directly causes the resonator to operate in a region with a reduced Q-factor. To prove this assumption in simulation, we inserted a 10 dB attenuator in the microstrip feedback path of Fig. 3(a), which effectively emulates an increased loss by the VTSDR. The PN simulated with this setup is shown in Fig. 6(b) and agrees well with the measurement result. This increased losses and the resulting unwanted shift to a non-optimal Q-factor can be compensated in a future revision of the chip, by increasing the loop gain with a third amplifier stage. Simulations taking these higher losses into account, using a measured high-Q on-chip spherical dielectric resonator model with the loss higher than 30 dB from [3], and having a higher gain due to an added third amplifier stage, predict an excellent PN of -114.8 dBc/Hz at 10 MHz offset from the oscillation frequency of 103.242 GHz. These results are shown by the red curve in Fig. 6(b).

IV. Conclusion

In this feasibility study, a concept for low phase noise silicon-based integrated voltage-controlled oscillator using high-Q self-aligned on-chip voltage-tunable spherical dielectric resonator was investigated, fabricated and measured. The designed resonator consists of a high-Q on-chip dielectric sphere and a tuning patch with varactors underneath it. An amplifier, which is combined with the proposed resonator as

TABLE I
COMPARISON WITH STATE-OF-THE-ART OF SILICON-BASED VCOS OPERATING ABOVE 90 GHZ

Ref.	**This work**	[5]	[6]	[7]	[8]
Tech.	**130nm SiGe**	65nm CMOS	65nm CMOS	130nm CMOS	130nm SiGe
Topology	**Spherical Dielectric Resonator**	Coupled Oscillators	Fund. Colpitts	Fund. Cross-Coupled	Push-Push
$f_{\text{osc,center}}$ (GHz)	**104.03**	105	98	91	103.5
Δf_{osc} (GHz)	**0.088**	9.975	8.64	0.455	25
$P_{\text{out,max}}$ (dBm)	**-9.9**	4.5	-1	4.5	4.2
PN @ 1 MHz (dBc/Hz)	**-76.4/ -92.3**[a]	-92.83	-90.85	-87	-108.7
PN @ 10 MHz (dBc/Hz)	**-95.9/ -114.8**[a]	-100[b]	-110.95	-107.7	-111[b]
P_{DC}^{c} (mW)	**32.5**	54	21.6	46	50

[a]: simulated with measured SDR, [b]: graphically estimated, [c]: with buffer.

a positive feedback, is designed to provide the oscillation. An output buffer is used to isolate it from the 50 Ω output load. In Table I, the proposed VCDRO is compared against the state of the art for LC tank based MMIC VCOs considering frequencies above 90 GHz. According to simulations based on measurements of all its blocks, after a simple redesign with increased loop gain, this oscillator can achieve a very promising PN of -114.8 dBc/Hz at 10 MHz offset.

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