230 GHz Signal Generator for High-Bandwidth Data Links in 130 nm SiGe BiCMOS

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***Abstract*—This study presents an analysis of an energy efficient signal generator designed to enable short-range wireless data links for innovative base station architectures. The focus of this research is to achieve efficient frequency generation at 230 GHz using 130 nm SiGe BiCMOS technology. The circuit consists of a 57.5 GHz fundamental oscillator followed by subsequent stages that quadruple the output frequency. The implemented design achieves an operating range from 208.7 GHz to 253.2 GHz with a maximum output power of 1.81 dBm. The DC-to-RF efficiency of the signal generator is measured to be 2.16 %, which is competitive with other signal generators in SiGe BiCMOS technology operating in this frequency range.**

***Index Terms*—Oscillators, frequency synthesis, voltage-controlled oscillator, quadrupler, millimeter wave, Sub-THz, BiCMOS integrated circuits, SiGe**

I. Introduction

Research into the fifth (5G) and sixth (6G) generations of mobile data communications is increasingly addressing concrete problems and scenarios [1]–[3]. In such ecosystems, edge cloud applications will play a critical role, enabling distributed computing and low latency applications [4], [5]. To support the dynamic nature of edge cloud services and to reduce overall energy consumption, baseband signal processing tasks can be efficiently completed by specialized compute nodes (CN) [3]. This enables highly energy-efficient, load-aware execution of the radio access network (RAN). As a result, the ability to dynamically switch high-speed data links between the CNs is of critical importance. In this context, a promising approach for distributing data can be the use of short-range, high-bandwidth wireless data links. An example of a system with four CNs is shown in Fig. 1. Each CN consists of a homodyne transceiver architecture and a specialized baseband processing unit. The aim of this work is to analyze a possible power-efficient signal generator with a center frequency of about 230 GHz needed as a local oscillator (LO) building block for such a data transmission link.

Designing oscillator circuits to generate fundamental frequencies above 200 GHz is a challenging task. It involves a complex trade-off between several key performance indicators (KPIs), including phase noise (PN), tuning range, DC-to-RF efficiency and center frequency. One way to address this challenge is to optimize each KPI with a dedicated building block. In the context of this paper, the most common approach is used. It consists of a fundamental voltage controlled oscillator (VCO) at a frequency of 57.5 GHz,

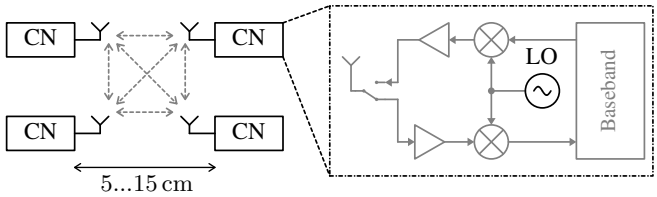

Fig. 1. Overview of the system with four compute nodes (CNs). Each CN consists of a conventional homodyne transceiver architecture, where the presented local oscillator (LO) circuitry is highlighted.

which is then multiplied by a factor of four using a phase controlled push-push (PCPP) frequency quadrupler. A buffered injection-locked oscillator (ILO) improves the spectral purity of the output signal and provides sufficient output power for subsequent mixers, modulators, and power dividers. In addition, the tuning range of the signal generator should be as reconfigurable as possible to allow channel selection in larger base-stations with multiple compute nodes by assigning data channels to widely separated carrier frequencies.

II. Signal Generator Design

To prove the concept, the monolithic integration is done in a 130 nm SiGe BiCMOS technology with heterojunction bipolar transistors (HBTs) having a maximum oscillation frequency $f_{\max}$ of 450 GHz. The high-frequency transmission lines (TL) are based on the concept of grounded coplanar waveguides, using the top metalization as the signal trace and one of the lower metal layers as ground. Each block is DC powered using a zero-ohm line approach [6]. A simplified schematic of the entire proposed signal generator is shown in Fig. 2.

The circuit topology of the fundamental VCO is based on a fully differential Colpitts oscillator architecture [7], [8]. The resonator consists of the inductive line $\mathrm{TL_{VCO}}$ and a binary-weighted capacitor bank, which is complemented by additional metal-oxide-semiconductor (MOS) varactors $\mathrm{C_{var}}$. This provides an analog continuous frequency tuning range (FTR) in addition to the digital configuration. For the resonator $\mathrm{TL_{VCO}}$, the grounded coplanar TL have been modified with a patterned ground plane. This minimizes losses and increases the quality factor by forcing the return current into the sidewalls of the TL. A common-base buffer-stage with HBT $\mathrm{T_2}$ is used to increase the load impedance seen by the oscillator core. The transistor $\mathrm{T_1}$ of the oscillator core is biased through $\mathrm{TL_{VCO}}$ by the high impedance $\mathrm{R_1}$. An interstage matching consisting of $\mathrm{TL_1}$, $\mathrm{TL_2}$ ensures optimal

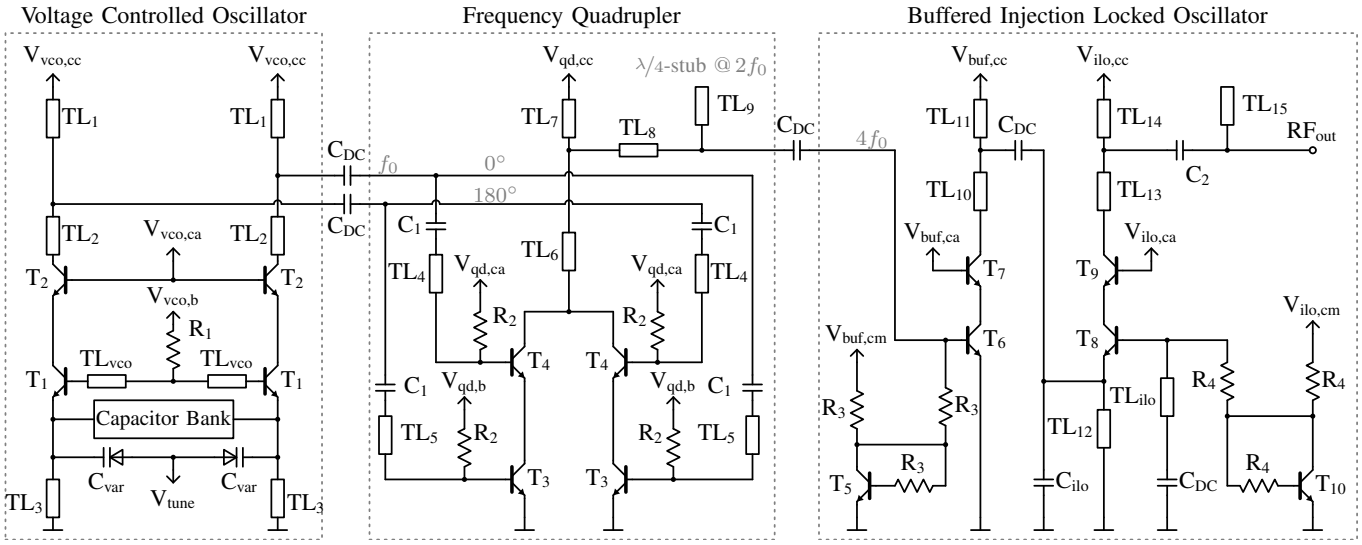

Fig. 2. Simplified circuit diagram of the proposed signal generator consisting of an oscillator, frequency quadrupler and injection locked oscillator.

power matching with the subsequent frequency quadrupler. This frequency quadrupler is used to up-convert the VCO output signal in frequency by a factor of four [9], [10]. To keep the power consumption and the total area of the chip as small as possible, this circuit consists of only two stacked HBTs T_3 and T_4 per path. The lower ones are class AB biased and the upper ones are class C biased. Building on the well established push-push principle for frequency multiplication-by-2, the single-stage frequency quadrupler employs the phase-controlled push-push architecture which allows a frequency multiplication-by-4 [10]. Input power matching of the transistors with different operating points is realized by TL_4, TL_5 and C_1. On the output side, the matching as well as the DC supply of this block is done by TL_6 and TL_7. A second harmonic suppression is realized by the $\lambda/4$ open stub line TL_9. To achieve higher output power and spectral purity, a buffered ILO is used [10]. The first buffer stage is realized in cascode topology consisting of T_6 and T_7 to amplify the quadrupled signal. This signal is then fed to the emitter node of the modified common-collector Colpitts oscillator as an ILO, which consists of the HBT T_8 and the resonant circuits TL_{ilo} and C_{ilo}. The free-running frequency of the ILO is 209 GHz. The quality factor of the resonator was intentionally chosen to be lower, as this results in a larger lock-in range of the ILO. Compared to a conventional oscillator, this would result in higher phase noise. With the ILO, however, the phase noise is only source-dependent [10]. Similar to the VCO circuitry with T_2, the HBT T_9 is used as an output buffer. The output matching of the overall signal generator was realized with the elements TL_{13}, TL_{14} and C_2 as well as TL_{15}.

III. Measurements

The signal generator has been characterized in a lab environment. As shown in Fig. 3, the chip is glued and bonded to a carrier board. This additional layer of wiring allows precise filtering of all supply voltages using decoupling capacitors, which is essential for characterizing individual

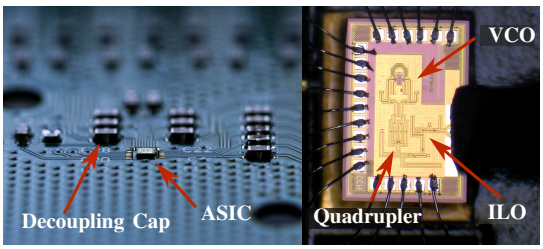

Fig. 3. Photographs of the chip glued and bonded to a carrier printed circuit board for RF measurements on a probe station while the DC power is supplied via the carrier board. The chip size is 810 µm × 1210 µm.

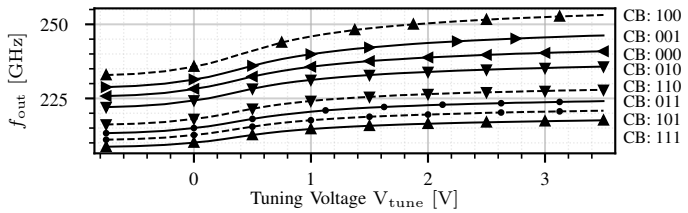

Fig. 4. Measured quadrupled output frequency f_{out} as a function of tuning voltage V_{tune} for different capacitor bank configurations (CB).

oscillators without using a phase-locked loop. The proposed circuit has been characterized using two different measurement setups attached to a spectrum analyzer. The first setup covers the frequency range of 140 GHz to 220 GHz and the second setup covers 220 GHz to 330 GHz. Power measurements are made with a power meter. All supply voltages were kept constant throughout the measurements, resulting in a total power consumption of 71.6 mW. The VCO consumed the most power with 52.8 mW.

Adjusting the tuning voltage V_{tune} from −0.5 V to 3.5 V results in the operating range shown in Fig. 4. Since the tuning characteristics overlap, it is also possible to use two different configurations for a given frequency, resulting in a possible switchable, segmented operating range of 208.7 GHz to 253.2 GHz. The corresponding continuous frequency tuning

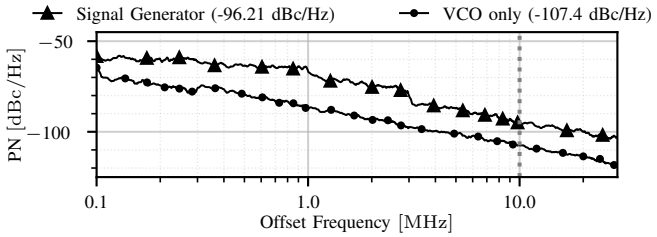

Fig. 5. Measured phase noise (PN) at an offset frequency of 10 MHz and as a function of the offset frequency for a tuning voltage $\mathrm{V_{tune}}$ of 0 V and for the entire signal generator as well as for the VCO only.

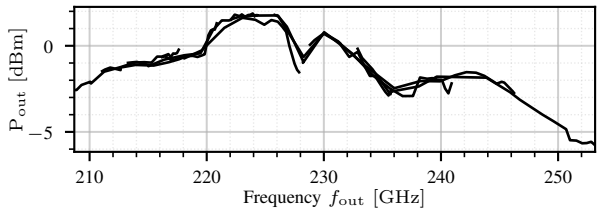

Fig. 6. Measured output power $\mathrm{P_{out}}$ as a function of the entire quadrupled output frequency f_{out} range for different capacitor bank configurations and tuning voltages $\mathrm{V_{tune}}$.

range varies between $4.15\,\%$ to $8.24\,\%$, depending on the selected capacitor bank configuration (CB), denoted by the 3 bits on the right. As shown in Fig. 5, the measured phase noise at an offset frequency of $10\,\mathrm{MHz}$ is $-96.21\,\mathrm{dBc/Hz}$ for a configuration of CB=000 and a tuning voltage $\mathrm{V_{tune}}$ of $0\,\mathrm{V}$. Compared to a measurement of a single VCO under the same operating conditions [8], the phase noise increases by $12\,\mathrm{dB}$, as expected from the theory. The measured output power of the signal generator as a function of the output frequency is shown in Fig. 6. The maximum output power is $1.81\,\mathrm{dBm}$ at a frequency of $222.4\,\mathrm{GHz}$. The losses caused by the measurement setup are calibrated. The resulting DC-to-RF efficiency is $2.16\,\%$. Tab. I summarizes the performance of the proposed signal generator and compares it to the state of the art. The presented circuit concept provides competitive KPIs for signal generators in SiGe technology in the $200\,\mathrm{GHz}$ range. This is shown by the figure of merit $\mathrm{FOM_T}$, a large negative value means an improvement in performance.

IV. Conclusion

This study analyzes an efficient signal generator for short-range data links for new base-station architectures. The goal was to provide efficient and reconfigurable frequency generation at $230\,\mathrm{GHz}$ using $130\,\mathrm{nm}$ SiGe BiCMOS technology to enable high-speed data distribution between specialized compute nodes within a base-station. The circuit consists of a $57.5\,\mathrm{GHz}$ fundamental oscillator, of which the output frequency is quadrupled by a subsequent stage. A maximum output power of $1.81\,\mathrm{dBm}$ is achieved over a segmented operating range of $208.7\,\mathrm{GHz}$ to $253.2\,\mathrm{GHz}$. The DC-to-RF efficiency of $2.16\,\%$ is competitive with other oscillators in this frequency range. The presented feasibility study indicates that the proposed concept is well suited for efficient and high performance data links for short range edge cloud applications.

TABLE I
Comparison to the state of the art in BiCMOS technology.

Ref.	f_0 [GHz]	PN [dBc/Hz]	$\mathrm{P_{out}}$ [dBm]	DC-to-RF [%]	$\mathrm{FOM_T}$ [dB]
[11]	190.5	-102.6‡	-2.1	0.21	-167.7
[12]	247.8	-81†	-2.6	1.3	-161.4
[13]	210	-87.5†	1.4	2.26	-178.0
[14]	251.0	-86†	-18	0.01	-153.3
This	230.92	-96.2‡	1.81	2.16	-172.5

Phase noise at 1 MHz (†) and 10 MHz (‡) offset Δf_{PN} to the carrier f_0. $\mathrm{FOM_T} = \mathrm{PN} - 20\log\left(f_0/\Delta f_{\mathrm{PN}} \cdot {}^{\mathrm{TR}}/_{10}\right) + 10\log\left({}^{P_{\mathrm{DC}}}/_{1\,\mathrm{mW}}\right) - \mathrm{P_{out}}$.

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