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AC performance tunability of flexible bottom gate InGaZnO TFTs by an additional top gate contact

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Abstract*—This study explores the performance tuning of flexible InGaZnO TFTs using a double gate configuration. DC analysis on individually controllable double gate TFTs highlights that the bottom gate biasing is highly effective in facilitating efficient switching of the devices, whereas the top gate biasing allows for controlling their performance. This is demonstrated for the AC response of the devices with different channel lengths showing the tunability of f_T and f_{MAX} with a maximum relative tuning up to $130\,\%$ for f_T and $170\,\%$ for f_{MAX}. A more efficient control is observed for longer TFTs, resulting in increased characteristics frequency up to $50\,\%$. Furthermore, the effect of the performance tunability is also reported even when the double gate TFTs are exposed to tensile strain induced by a bending radius of $2\,\mathrm{mm}$. These findings indicate new possibilities towards the design of flexible analog systems with dynamically adjustable performance.

***Index Terms*—Flexible electronics, InGaZnO, Thin-Film Transistors, Transit frequency, Double-gate TFTs**

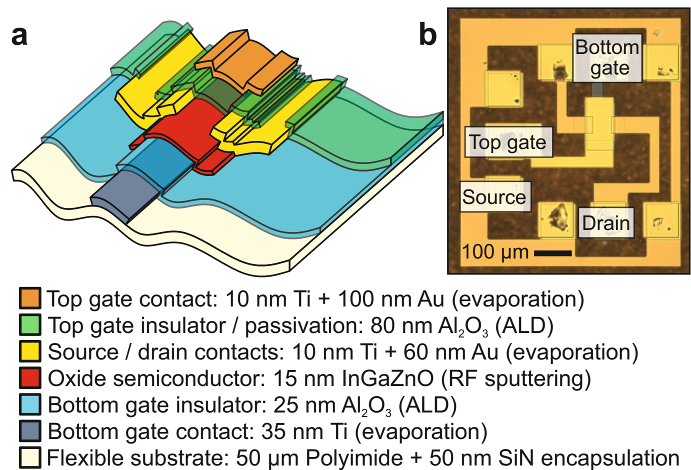

Fig. 1. Flexible IGZO double gate TFTs: a) Device structure. b) Device micrograph.

I. Introduction

THIN-film electronics on unconventional substrates can be flexible, stretchable, transparent, and/or lightweight [1], [2]. Such properties promise the realization of new applications ranging from smart textiles [3] to unobtrusive biocompatible sensor tags [4]. However, the performance of flexible electronic devices can not yet meet the requirements of most of these systems. In particular, thin-film transistors (TFTs) for sensor readout systems have to be reliable, compatible with large-area manufacturing systems, and fast enough to realize analog circuits for conditioning amplifiers and communication circuitry. A common metric to rate the AC performance of TFTs is their transit frequency f_T. While there are examples of flexible nanoscale TFTs with transit frequencies above $10\,\mathrm{GHz}$, these devices normally utilize non-scalable fabrication techniques, such as electron beam lithography [5], or exotic semiconductors, such as MoS_2 [6].

A promising TFT technology for the realization of flexible analog circuits are transistors based on amorphous InGaZnO (IGZO) as they combine large-area and low-temperature manufacturability with excellent electrical and mechanical properties [7], [8]. Besides the choice of materials, the geometry of TFTs has a significant influence on their AC performance. The obvious approach is to use short channels to increase transconductance and f_T [9]. However, TFTs fabricated on flexible free-standing substrates suffer from misalignment issues and parasitic capacities caused by overlapping due to substrate deformation during the fabrication process, which are more relevant for small devices, i.e., short channel TFTs [10]. Nevertheless, also the use of multi-gate structures has been proven to be useful in improving the performance of flexible oxide-based devices and circuits. Additional gates in TFTs can modulate the threshold voltage [11], [12], enable unipolar circuits with CMOS-like operation principles [13], improve the electrical stability of transistors [14], reduce mechanical strain [15], be used for sensing applications [16], influence the noise performance [17], and also increase their on/off ratio and

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effective mobility [18]. However, the AC performance of such devices has not been sufficiently investigated. So far it has only been shown that double gate TFTs with connected top- and bottom-gates (resembling a single gate all around) exhibit an improved f_T compared to standard bottom gate TFTs [19]. Here, the influence of an individually controllable top gate on the AC performance of bottom gate TFTs is presented. The devices are shown in Fig. 1 and are used to evaluate the new concept of dynamically tuning the transit frequency of flexible double gate IGZO TFTs.

II. Device Structure and Fabrication

All devices were manufactured on free-standing $7.4\,\mathrm{cm} \times 7.4\,\mathrm{cm}$ large and $50\,\mu\mathrm{m}$ thick polyimide foil utilizing a three metal layer process optimized for the realization of flexible integrated circuits [20]. The TFTs utilize a Ground-Signal-Ground pad layout to enable reliable AC measurements.

Fig. 1a illustrates the layer structure and materials used. The fabrication never exceeds a temperature of $150\,°\mathrm{C}$, and is based on standard UV lithography. It started with the encapsulation of the polyimide substrate with $50\,\mathrm{nm}$ PECVD grown SiN_x. Next, $35\,\mathrm{nm}$ Ti were evaporated and structured into bottom gates. These gates were insulated by $25\,\mathrm{nm}$ thick Al_2O_3 (ALD) [21]. Then, $15\,\mathrm{nm}$ of IGZO were RF sputtered from a ceramic $InGaZnO_4$ target and both layers were individually structured by wet etching. Next, the source and drain contacts were formed by evaporated and structured $10\,\mathrm{nm}$ Ti + $60\,\mathrm{nm}$ Au. $80\,\mathrm{nm}$ thick Al_2O_3 was grown by ALD and structured simultaneously to act as a passivization and top gate insulating layer. Finally, $10\,\mathrm{nm}$ Ti + $100\,\mathrm{nm}$ Au were evaporated and structured by lift-off to form the top gate contact having the same gate-to-source/drain overlap as the bottom gate contact. Fig. 1b shows a micrograph of a fully processed double gate TFT.

III. Results and Discussion

The TFTs were characterized under ambient conditions using a Keysight B1500A parameter analyzer to measure their DC performance and provide bias voltages, and a two-port Keysight E5061B ENA vector network analyzer to quantify the AC properties.

A. DC performance

A full set of representative (1 out of 57 measurements) DC characteristics for a double gate TFT with a channel length over width ratio of $50\,\mu\mathrm{m}/50\,\mu\mathrm{m}$ is shown in Fig. 2. The TFT was measured in both bottom gate and top gate operation (Fig. 2a), by always applying a DC voltage on the second gate to tune the performance. The electrical parameters, extracted using the Shichman-Hodges model [22], exhibited effective mobility, on-off current ratio, and subthreshold swing values up to $16.6\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$, 1×10^8, and $120\,\mathrm{mVdec}^{-1}$, while the gate leakage current stayed below $10^{-10}\,\mathrm{A}$ for all measurements. Capacitance measurements for both the top gate and bottom gate operation of the TFT are shown in Fig. 2b. The frequency dependency of the capacitance is typical for TFTs with comparable geometry and linked to the fact that charges

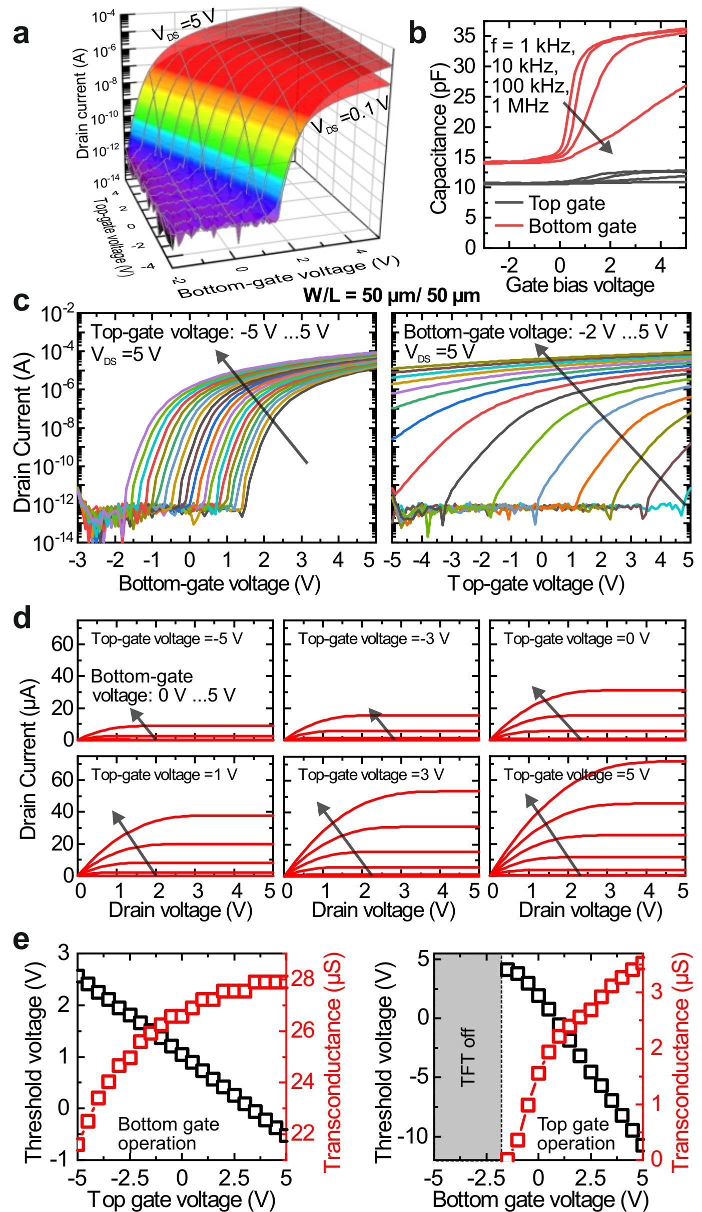

Fig. 2. Double gate TFT DC performance: a) TFT transfer characteristics dependency on top- and bottom-gate voltage. b) Comparison of top- and bottom-gate capacitance (all other contacts grounded). c) Threshold voltage variation caused by the top and bottom gate. d) Representative bottom gate output characteristics for different top gate voltages. e) Variation of the threshold voltage and transconductance for bottom- and top-gate operation. All voltages are measured relative to the grounded source contact.

cannot be efficiently injected into the semiconductor layer at high frequencies [23]. The graph shows that the difference in gate capacities for the two gates is mainly related to the difference in the gate insulator layer thickness of the bottom and the top gate ($25\,\mathrm{nm}$ and $80\,\mathrm{nm}$, respectively), but can also be influenced by the unavoidable annealing treatment of the bottom gate insulator layer during the top gate layer growing.. While the capacitance of the bottom gate reaches values of $4.1\,\mathrm{mF\,m}^{-2}$ (calculated considering the size of the gate, the overlaps, and the semiconductor island size), the corresponding value for the top gate is only $1.4\,\mathrm{mF\,m}^{-2}$. These results

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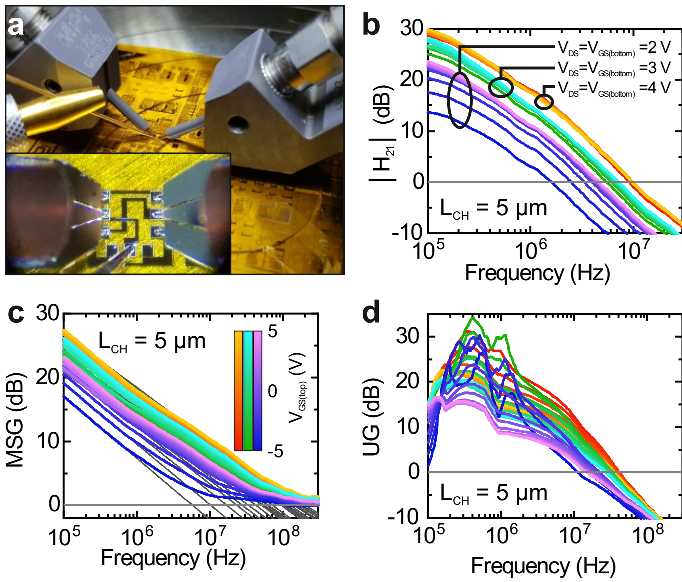

Fig. 3. AC measurements of flexible double gate TFTs: a) contacted double gate TFT with 5 µm channel length. b)-d) Absolute value of current gain (h_{21}), maximum stable gain (MSG), and unilateral gain (UG) extracted from S-parameters. All parameters are measured at bias voltages of V_{DS}=$V_{GS(bottom)}$ =2 V, 3 V, and 4 V, and top gate voltages $V_{GS(top)}$ between −5 V and 5 V.

highlight that the electrostatic control of the bottom gate over the channel is dominant. Hence the bottom gate can be used to efficiently switch the TFT, while the weaker coupling of the top gate is suitable to tune the threshold voltage of the TFT. This is illustrated in the TFT transfer characteristics in Fig. 2c, showing that the dominant bottom gate is always able to control the TFT while the top gate voltage between −5 V and 5 V can shift the effective threshold voltage from 2.6 V and −0.5 V. In the case of top gate operation the TFT can only be turned on for bottom gate voltages above −1.5 V, and at the same time remains mostly on for all bottom gate voltages above 2.5 V. Consequently, the top gate should only be used to adjust the TFT performance for bottom gate operation. To complete the TFT DC characterization, Fig. 2d displays a selection of representative output characteristic plots showing the TFT under bottom gate operation measured at various static top gate voltages. The measurements are in line with the shown transfer characteristics and illustrate the saturation behaviour of the device. Finally, a direct comparison of the performance parameters of the same transistor for top and bottom gate operation is given in Fig. 2e. The graph displays a close-to-linear tunability of the threshold voltage, and also the significantly higher maximum transconductance g_m of the TFT when operated using the bottom gate. At the same time, it shows that g_m can be adjusted to any value between 21.6 µS and 27.9 µS, which is crucial when the AC performance of the device is tuned by the top gate voltage.

B. AC performance

AC characterization of DG TFTs was carried out by using two GSG probes to contact the drain and the bottom gate pads, and an additional DC probe to set the bias voltage on

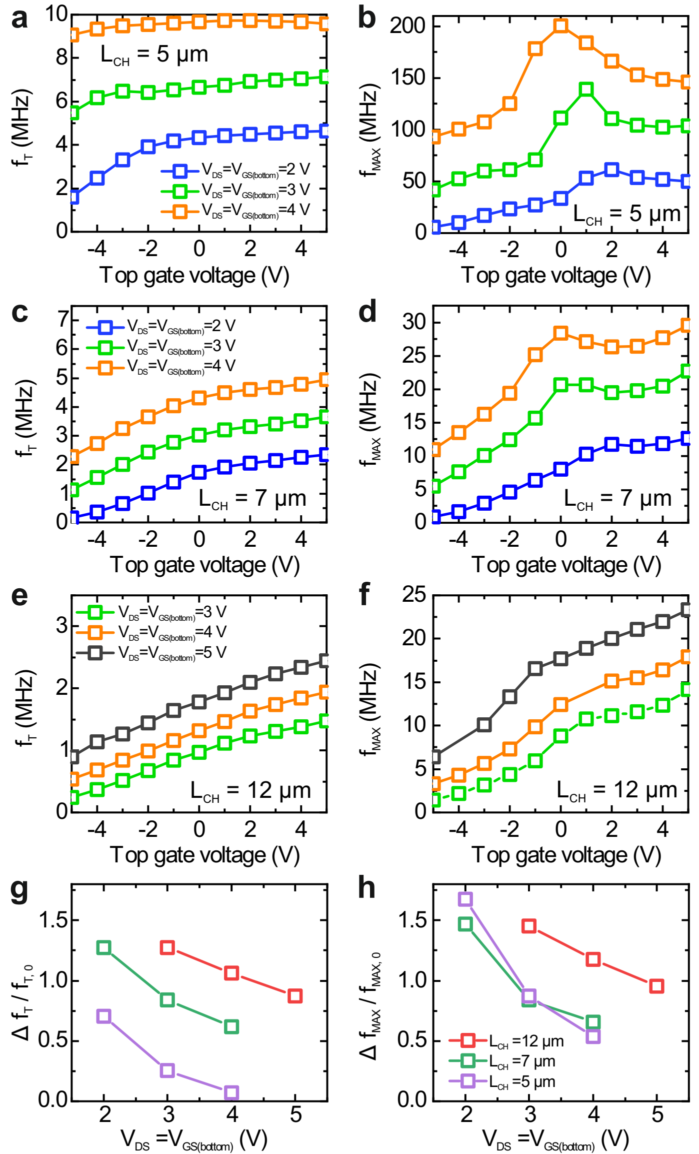

Fig. 4. Top gate voltage dependency of TFTs AC performance: a) Transit frequency and (b) maximum oscillation frequency of a 5 µm long TFT for different bias voltages and top gate voltages. c) and (d) same measurements for a 7 µm long TFT. e) and (f) corresponding measurements for a 12 µm long TFT. g) and (h) relative tunability of the transit frequency and maximum oscillation frequency at top gate voltages between −5 V and 5 V for TFTs with channel lengths of 5 µm, 7 µm, and 12 µm.

the top gate. This setup allowed for measuring the scattering parameters at different bias points of the top gate as shown in Fig. 3a. TFTs with channel length L_{CH} of 5 µm, 7 µm and 12 µm were measured. The two shorter TFTs were characterized for bias voltages of V_{DS}=$V_{GS(bottom)}$ =2 V, 3 V, and 4 V, whereas the 12 µm-long TFT was characterized for bias voltages of V_{DS}=$V_{GS(bottom)}$ =3 V, 4 V, and 5 V. For all the measurements, the applied top gate voltage $V_{GS(top)}$ was between −5 V and 5 V. The acquired S-parameters were used to calculate the frequency-dependent absolute value of the current gain h_{21}, the maximum stable gain MSG, and the unilateral gain UG [24]. Representative results for a 5 µm-long TFT are shown in Figs. 3b, 3c and 3d, respectively. Based on

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h_{21}, MSG, and UG the transit frequency f_T (defined as the unity current gain frequency), as well as f_{MAX} (either defined as the unity gain frequency of MGS or GU) of the TFTs were extracted. These frequencies quantify the maximum frequency up to which the device can provide current and power gain. The resulting values for f_T and f_{MAX}, extracted for different channel lengths and bias voltages, are plotted in Fig. 4. As expected f_{MAX} is constantly higher than f_T [25], and both values strongly depend on the channel length of the TFTs. Furthermore, the measurement shows that top gate biasing can actually tune the AC performance of the flexible TFTs as f_T and f_{MAX} reduced when top gate voltages went from higher to lower values. This is consistent with the modulation of the transconductance of the devices by the top gate voltage. Additionally, f_T and f_{MAX} values at positive top gate bias voltages are higher than those at $0\,\mathrm{V}$, suggesting that better AC performance can be achieved than that of comparable bottom-gate TFTs. The consistent initial rise followed by a decline in all f_{MAX} values indicates that higher voltage can push the short-channel devices out of their optimal saturation regime, worsening the well-known challenge of misalignment in short devices which reduces their output resistance and hence affects their frequency performance. This observation suggests that AC performance tuning is generally more efficient for longer TFTs, showing an increase of f_T as well as f_{MAX} by around $50\,\%$. This is explained by the fact that longer TFTs are relatively less affected by misalignment than shorter TFTs, and the longer channel length still ensures that the two gates overlap over most of the channel area, even when not fully aligned, allowing the control of the device and its performance tunability. A comparison of the impact of the top gate voltage on TFTs in relationship with their different channel lengths is reported in Fig. 4g and 4h, respectively, showing a maximum tunability of f_T and f_{MAX} for each bias point up to $\approx 130\,\%$ for f_T and $\approx 170\,\%$ for f_{MAX} compared to the frequencies values obtained at $V_{GS(top)}$ of $0\,\mathrm{V}$. The graphs also display a different effect of the top gate biasing with the channel length. Fig. 4g shows a consistent variation of f_T for each channel length due to the transconductance variation with the top gate biasing. On the other hand, Fig. 4h displays an outlier for the shortest TFT at the lower bias because of the dependence of f_{MAX} from both the transconductance and the output resistance (not affecting the f_T) [10], [26], which is higher at lower bias voltage and quickly drops down at higher bias voltage (device entering in saturation region). The combination of both the effect of the top biasing and the misalignment with the channel length enables the use of longer TFTs, easier to fabricate than shorter ones, for high-frequency and analog applications.

Additionally, it is worth mentioning that the top gate voltage also influences the static power consumption of the TFTs, as evident from Fig. 2. Consequently, the additional degree of freedom provided by the top gate contact enables the dynamic tuning of the performance of TFTs for analog circuits while optimizing energy consumption and bandwidth.

C. Flexibility

While the influence of bending on the DC and AC performance of flexible IGZO TFTs has been investigated in the past [27], the flexibility of double gate TFTs was explored in the DC domain [12], [18], [28], or for TFTs with connected top- and bottom-gates [19]. Therefore, it is important to ensure that the described tunable devices stay functional when exposed to mechanical strain. Fig. 5a shows the device when bent as well as representative measurements of the current gain (Fig. 5b) and the maximum stable gain (Fig. 5c) of a double gate TFT while flat and bent. The measurement demonstrates that the TFTs stay fully functional when bent to a radius of $2\,\mathrm{mm}$. This deformation corresponds to a tensile mechanical strain of $\approx 1.25\%$ parallel to the channel [29]. Traditionally, TFTs with similar layer structures can withstand a comparable bending radius of $1.7\,\mathrm{mm}$ [30] [9]. The flexibility test was done for different bending radii of $12\,\mathrm{mm}$, $8\,\mathrm{mm}$, $5\,\mathrm{mm}$, $4\,\mathrm{mm}$, $2\,\mathrm{mm}$, and $1.5\,\mathrm{mm}$. The device, however, failed to function at a $1.5\,\mathrm{mm}$ bend radius due to an excessive tensile strain. The individual current gain measurements of the DG TFT are shown in Fig. 5d. The plots show measurements for V_{DS}=$V_{GS(bottom)}$ $=4\,\mathrm{V}$, and top gate voltages $V_{GS(top)}$ of $-5\,\mathrm{V}$, $0\,\mathrm{V}$ and $5\,\mathrm{V}$. The extracted values for f_T and f_{MAX} visualized in Fig. 5d confirm the nearly negligible influence of mechanical strain on the frequency performance of flexible IGZO TFTs specifically at smaller tensile strains which was known from previous investigations [30]. This exemplifies that the tunability of the double gate is not negatively impacted by bending. Strain changes the maximum relative f_T tuning range from $\approx 143\,\%$ to $\approx 60\,\%$, and the maximum relative f_{MAX} tuning range from $\approx 117\,\%$ to $\approx 64\,\%$. In all cases, the positive effect of the top gate biasing is illustrated by the fact that the cutoff frequencies demonstrated at $V_{GS(top)}$ $=5\,\mathrm{V}$ exceed the values obtained without or negative top gate bias voltage.

IV. Conclusion

The implementation of a double gate configuration for tuning the performance of flexible IGZO TFTs is presented. The top gate bias control over the TFTs performance is already suggested from the DC characterization and further demonstrated with the analysis of the frequency response. A maximum relative tuning up to $130\,\%$ for f_T and $170\,\%$ for f_{MAX} is obtained by applying a static voltage to the top gate from $-5\,\mathrm{V}$ to $5\,\mathrm{V}$. This proves that the AC performance of IGZO TFTs can be controlled by using the top gate contact compared to bottom gate TFTs performance, i.e., top gate voltage equals $0\,\mathrm{V}$. The tunability of the AC performance is guaranteed even when the devices are bent to a radius of $2\,\mathrm{mm}$. Furthermore, the performance control by top-gate biasing is more effective on longer TFTs and affected by relatively less misalignment between the top and the bottom gate, resulting in an increase of the characteristics frequencies of about $50\,\%$. The results showcase the double gate configuration as a suitable design for controlling the AC performance of IGZO TFTs and indicate new possibilities concerning the realization of flexible analog circuits.

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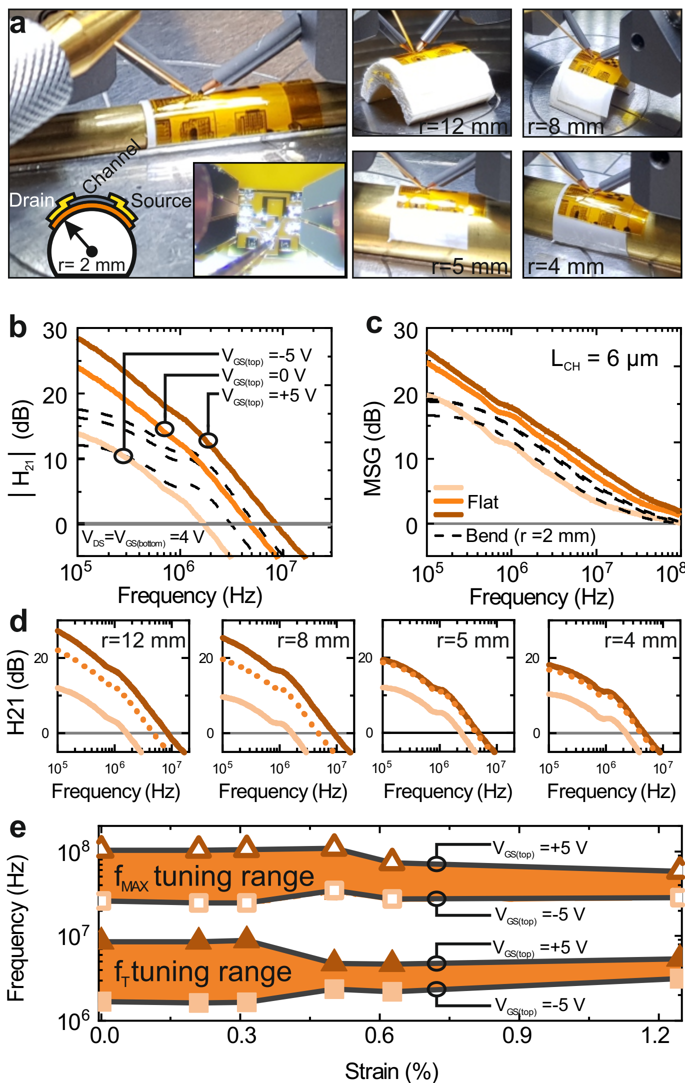

Fig. 5. Bendability: a) Photograph of bent and contacted flexible double gate TFTs at different bending radii: 12 mm, 8 mm, 5 mm, 4 mm, and 2 mm. b) Absolute value of the current gain, and c) maximum stable gain of a flexible double gate TFT while flat and bent to a tensile radius of 12 mm. The device was measured for V_{DS}=$V_{GS(bottom)}$ =4 V, and top gate voltages $V_{GS(top)}$ of −5 V, 0 V and 5 V. d) Absolute value of the current gain of the double gate TFT at tensile radius of 12 mm, 8 mm, 5 mm, and 4 mm. e) Resulting transit frequencies and maximum oscillation frequencies versus strain (radii: 12 mm, 8 mm, 5 mm, 4 mm, and 2 mm).

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