8.0 pJ/bit BPSK Transmitter with LO Phase Steering and 52 Gbps Data Rate Operating at 246 GHz

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***Abstract*—This work investigates a broadband binary phase-shift keying (BPSK) transmitter system with a measured data rate of 52 Gbps and 8.0 pJ/bit transmitter efficiency. The transmitter features local oscillator (LO) multiplication, 360° LO phase steering for phased array applications, a power-efficient BPSK modulator, and a very compact power amplifier connected to a differential bond wire interface. By employing a low-order modulation scheme, the baseband chain can be implemented at a very low complexity, which benefits power consumption. Proving the concept, an integrated circuit is fabricated in a 130-nm silicon–germanium (SiGe) bipolar complementary metal–oxide–semiconductor (BiCMOS) technology with a f_t/f_{max} of 350/ 450 GHz, covering 1.158 mm^2. At 52 Gbps, this circuit shows the highest reported data rate using BPSK modulation. The saturated output power of 3.5 dBm, while consuming 414 mW of direct-current (DC) power, results in a radio-frequency (RF) efficiency of 0.54%, which is a 28% improvement versus the state of the art. The high achieved data rate combined with circuit modules optimized for low power consumption results in a measured transmitter efficiency of 8.0 pJ/bit, improving the state of the art of complete transmitter systems in the same frequency band by 68% and 46% compared to BPSK and quadrature phase-shift keying (QPSK) systems respectively.**

***Index Terms*—Binary phase shift keying (BPSK), Broadband circuits, Phased arrays, Ultra wideband communication.**

I. Introduction

With an ever-increasing volume of transmitted data and the continuous growth of the Internet and Internet-of-Things (IoT)-based applications comes a need for higher data rate links and low-power systems providing the infrastructure for this. In the widely used frequency ranges below 10 GHz, this is achieved by high-order modulation schemes like quadrature amplitude modulation (QAM) digital-to-analog (DAC) and analog-to-digital (ADC) chains with massive digital processing consuming large DC power to achieve the targeted data rates. Ultimately, the available spectrum and mobile computing capabilities are the limiting factors. Due to the advancements in silicon and silicon-germanium technologies featuring devices with a f_{max} over 300 GHz, new frequency bands and applications above 100 GHz open up. At these frequencies, channel bandwidths of tenths of gigahertz are possible. Therefore, research and industry are looking into higher operating frequencies.

One of the key challenges of these systems is free space path loss. Compensating this necessitates high output powers together with high-gain antennas or antenna arrays. However, this also offers a possible benefit in increasing spacial diversity for chip-to-chip, chip-to-board, and femtocell mobile networks scenarios enabling many transmitters nearby on the same frequency band without the use of complex modulation or network protocols.

Exploiting the bandwidth requires adequate system topologies. Simpler approaches employ on-off-keying (OOK) [1], [2] or binary phase-shift keying (BPSK) [3], [4]. Higher order modulation systems using IQ-transceivers were demonstrated with data rates up to 120 Gbps [5]–[7]. While IQ-systems seem superior at first glance, an important question remains: How to generate the symbols in the baseband (BB) circuitry? While some approaches show the feasibility of high order IQ modulation in a more power efficient way [8], commonly high data rate complex symbols necessitate power-hungry and costly DAC and ADC systems. At the same time, binary data streams are readily available in all forms of modern systems with data rates exceeding 50 Gbps. Further, the demodulation of a BPSK signal is significantly easier and, therefore, more power efficient compared to complex modulation. This is exemplified by a very simple 1-bit analog-to-digital converters (ADC) being sufficient in the receive path [9].

This research work focuses on designing a very broadband transmitter enabling BPSK communication and exploiting the large available bandwidth in the mm-wave spectrum with data rates up to 56 Gbps. Limiting the circuit to a low-order modulation scheme can significantly reduce the design complexity in the baseband chain. Further, by reducing

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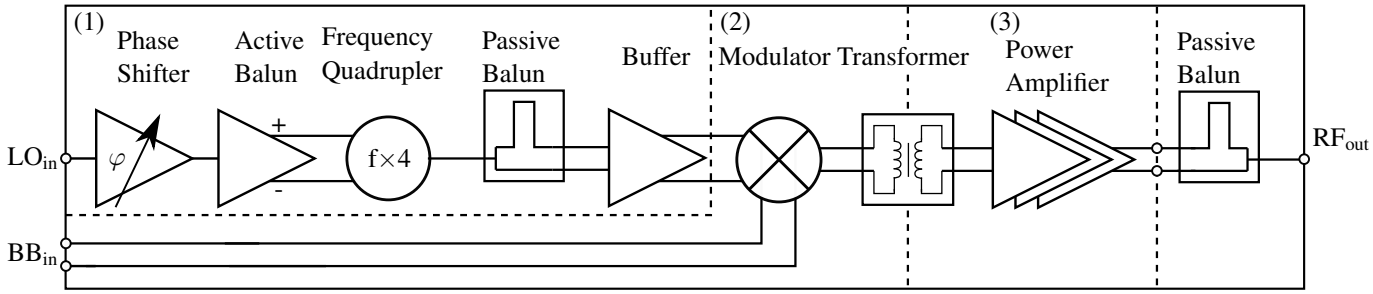

Fig. 1. Simplified architecture of the proposed transmitter system. It features (1) a LO chain , consisting of a phase shifter [10], an active balun [11], a frequency quadrupler [11], [12] and a differential buffer, (2) a BPSK modulator [13] and (3) a power amplifier [14] stage.

the circuit elements in the radio-frequency (RF) path, both chip area and power consumption can be optimized. Including phase steering in the LO-path and minimizing the width of the layout allows the flexible combination of many transmitters in a dynamically steerable antenna array. At the same time, high channel frequencies improve spacial diversity in this frequency band, inherently alleviating channel congestion.

This paper investigates the transmitter chip itself without an antenna to pave the way for modular systems featuring different outputs, by employing novel packaging concepts [15]. This enables the separate characterization of all components avoiding the superposition of behaviors in transceiver systems. Further, the limitations of transmitter measurements with commercially available measurement equipment are discussed. The proposed transmitter architecture is presented in section II. Transistor level schematics and key design considerations of the main modules are described in section III. Section IV describes small-signal, large-signal, and transmission simulation, as well as measurement results. Finally, the achieved performance is summarized and compared to the state of the art in section V.

II. Architecture

The proposed transmitter system, shown in Fig. 1, consists of three major sections: (1) A local oscillator (LO) chain, (2) a BPSK modulator, and (3) a power amplifier (PA).

An externally generated $61.5\,\mathrm{GHz}$ LO signal is supplied to a 90° phase shifter [10]. The system can later be integrated further with adequate signal distribution networks and established integrated voltage-controlled oscillators [16]. The phase shifter's high gain eases the LO signal supply by allowing low signal power levels of less than $-15\,\mathrm{dBm}$. Controlling the phase of the LO signal enables LO chain based beam steering [17]. The advantage of this approach is the reduction of complexity in the RF path and allows a more narrow band design of the phase shifter circuit, thus, enabling higher gain and output power of this stage. This enables dynamic beam steering when multiple transmitters are combined in an antenna array.

The phase-shifted single-ended signal is then converted to a differential signal and further buffered by an active balun based on an asymmetrically fed differential cascode with capacitive phase and magnitude imbalance correction [11].

The differential signal is crucial for feeding the frequency quadrupling stage. Extending the established push-push architecture [18], a phase-controlled push-push architecture [11], [12] enables the frequency multiplication by four in a single stage resulting in a compact and low-power design. Here, the $61.5\,\mathrm{GHz}$ input signal is up-converted to the target center frequency of $246\,\mathrm{GHz}$. As the frequency is the derivative of the phase, multiplying the frequency inherently results in the multiplication of the phase as well, according to [10]

$$n \cdot \varphi = n \left(\int_T 2\pi f t dt \right) = 2\pi (n \cdot f) t + n \cdot \varphi_0. \qquad (1)$$

This has been practically shown in [19]–[21]. It is, therefore, possible to achieve $360°$ of phase control in the target band and precise beam steering in large array systems.

Concluding the LO chain, the signal is buffered by a pseudo-differential based amplifier stage to achieve suitable signal power levels to optimize the modulator performance. In total the LO chain is designed to produce $-1.5\,\mathrm{dBm}$ of power at the center frequency of $246\,\mathrm{GHz}$.

The modulator is designed with a focus on maximum bandwidth for BPSK operation to maximize the data rate [13]. Driving the power amplifier into saturation with moderate baseband input powers of $-12\,\mathrm{dBm}$ the modulator is designed to output $-10.4\,\mathrm{dBm}$ at $52\,\mathrm{GHz}$ of RF bandwidth.

A three-stage power amplifier is connected via a transformer. Its multi-stage design combines a large bandwidth with a high gain and simulated output power of more than $0\,\mathrm{dBm}$ [14].

A passive balun was added to allow single-ended probing in the research laboratory. It is connected via an on-chip GSSG bond interface [15] and can be replaced with an antenna.

III. Circuit Design

This section describes the circuit components of the phase shifter, frequency quadrupler, modulator, and power amplifier functional blocks.

A. 60 GHz Vector-Sum Phase Shifter

The externally generated local oscillator (LO) signal is fed to an active vector-sum quadrature phase shifter [10] shown in Fig. 2. A broadside coupler creates the necessary quadrature signals. It produces small attenuation of less than $1\,\mathrm{dB}$, while the area penalty is limited due to small passive structures at $60\,\mathrm{GHz}$. The I and Q signals are weighed by symmetrical

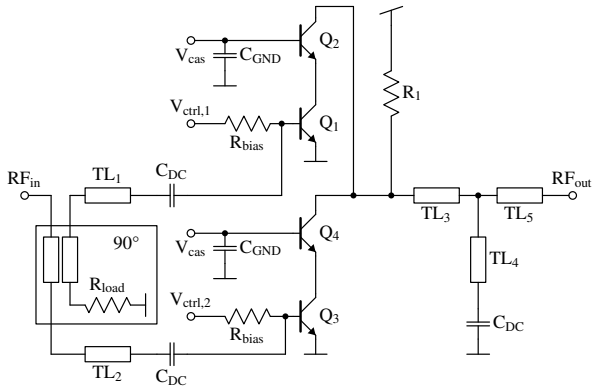

Fig. 2. Simplified schematic of the vector-sum phase shifter operating at 60 GHz.

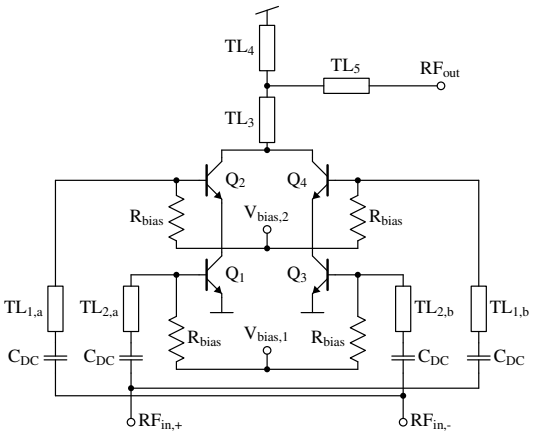

Fig. 3. Simplified schematic of the proposed frequency quadrupler.

variable gain amplifiers (VGA). These are built as cascodes for high gain and reverse isolation improving the phase steering precision. The transistors are twice the unit size [22], trading off power consumption and output power. A resistive load and a transmission line based interstage matching combine high gain with high output power, enabling direct feeding of the frequency quadrupling stage while limiting the overall area. Supplied at 2.6 V and with both VGAs at the same operation point, this circuit consumes 8.84 mW. The phase can be controlled via a single tuning voltage which is fed to a differential stage supplying the actual DC biasing to the VGAs while consuming an additional 4.4 mW. In complex, integrated systems, this avoids one entire DAC, which can reduce design complexity and overall power consumption. The gain can be tuned via the bias point of the DC circuitry. This is usually not necessary as LO chains are commonly designed to drive the modulator circuit for maximum output power.

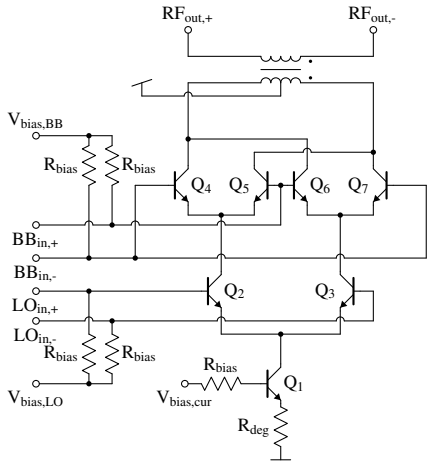

Fig. 4. Simplified schematic of the employed broadband modulator.

B. Phase-Controlled Push-Push Frequency Quadrupler

Depicted in Fig. 3 is the phase-controlled push-push based frequency quadrupler [11], [12]. Building on the established push-push architecture used for frequency doubling [23], this circuit type enables frequency multiplication by four in a single stage [24]. This is achieved by stacking two differential stages $Q_{1,3}$ and $Q_{2,4}$, where the first stage is biased in class AB and the upper stage operates in class C. The signal input power level and bias points must be carefully chosen and the inputs of both stages must be matched separately to optimize the signal phases in the frequency multiplication core. The operation points are set at 0.89 V and 1.95 V with all transistors scaled to two times the unit transistor size [22]. The preceding active balun is connected via DC-decoupling capacitors. Special care was taken to the signal crossings and line geometries connecting the separate transistors to maximize the fourth harmonic signal while minimizing all spurious harmonics by using extensive electromagnetic modeling and simulation. The main advantage of this architecture is the low power consumption resulting from re-using the collector current in both stacked stages. As a result, the circuit is uses only 19.2 mW from a 2.4 V supply during operation in simulation.

C. Broadband Gilbert-Cell Modulator

Fed by a differential buffer, a Gilbert-cell, shown in Fig. 4, is used as the BPSK modulator [13]. While transistors $Q_{4,\ldots,7}$ are unit size transistors [22], optimizing for both maximum transit frequency and power consumption, $Q_{2,3}$ are twice as large and Q_1 is scaled by n=4. The operation point is set by Q_1, which features an emitter degeneration for improved bias stability. With the baseband signal fed to the upper transistors, the Gilbert cell operates similarly to a differential cascode amplifier for the LO signal during each bit period. This is advantageous because of the reduced Miller effect and, thus, increased gain in the LO path. A transformer matches the output of the modulator to the input impedance of the following power amplifier stage and feeds the 3.6 V supply voltage via a center tap. Including the bias structures, this circuit consumes 35 mW.

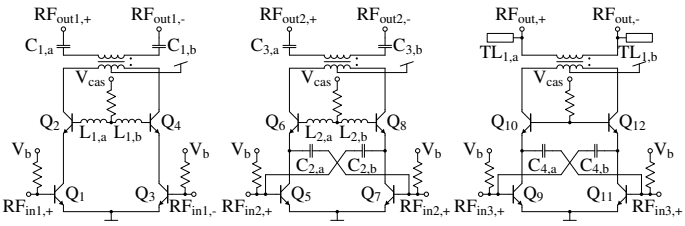

Fig. 5. Simplified schematic of the output power amplifier.

D. Three-Stage Power Amplifier

The power amplifier, depicted in Fig. 5, consists of a three-stage pseudo-differential cascode design with frequency staggering of the stages and transformer coupling [14]. The cascode topology is employed due to the reduction in the miller effect and thus enhancing broadband operation. The first stage transistors $Q_{1,\ldots,4}$ are four times the unit size [22] to reduce power consumption and input capacitance. Base inductors L_1 of the upper-stage transistors enhance the frequency response [25]. Although the transformer provides DC decoupling, additional capacitors C_1 are used to tune the frequency response of the inductance of the transformer with the base capacitance of the transistors. The second stage uses eight times the base transistor size [22] to provide enough output power for the last stage. In addition to the base inductors L_2 in the upper stage, capacitive neutralization by MOM capacitances C_2 is employed to reduce the base capacitance further. The last stage is tuned for maximum output power and uses capacitive neutralization C_4 without base inductances on the upper transistors. The output is transformer coupled and matched to the $100\,\Omega$ differential impedance by two $20°$ long $25\,\Omega$ open stubs. All stages are biased by duplicated bias networks placed symmetrically next to the stages. The PA covers an area of $300\,\mu\text{m} \times 150\,\mu\text{m}$ and consumes $251.1\,\text{mW}$ from a $3.3\,\text{V}$ supply. A main design goal is to achieve very wideband operation from $210\,\text{GHz}$ to $300\,\text{GHz}$, however it was found that small signal analysis alone is not sufficient in the design process. Multi-tone large-signal simulations showed severe interference effects possibly limiting wideband, large-signal operation close to the saturation. Overcoming this, small signal gain and flatness was trade-off for an improved large signal wideband characteristic.

IV. Simulation and Measurement Results

To prove the concept, the proposed architecture is realized in a state-of-the-art $130\,\text{nm}$ SiGe BiCMOS technology with $f_T/f_{max} = 350/450\,\text{GHz}$ [22]. A microphotograph of the fabricated integrated circuit (IC) is shown in Fig. 6. The entire chip measures $837\,\mu\text{m}\times1920\,\mu\text{m}=1.6\,\text{mm}^2$, including a passive balun, which can be connected via differential wire bonding, allowing probing in the research laboratory. This section can be diced off and replaced by different antenna structures. The actual transmitter measures $1514\,\mu\text{m}\times765\,\mu\text{m}=1.158\,\text{mm}^2$, with the pads consuming almost $40\,\%$ of the area. During operation, the circuit consumes a total of $413.9\,\text{mW}$ splitting into $127.7\,\text{mW}$ for the phase-steering LO chain, $33.9\,\text{mW}$ for the modulator and $251.1\,\text{mW}$ for the three-stage power amplifier.

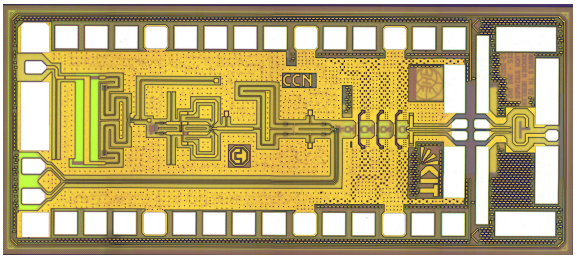

Fig. 6. Microphotograph of the manufactured transmitter circuit. The chip measures $837\,\mu\text{m}\times1920\,\mu\text{m}=1.6\,\text{mm}^2$ while the transmitter consumes $1514\,\mu\text{m}\times765\,\mu\text{m}=1.158\,\text{mm}^2$.

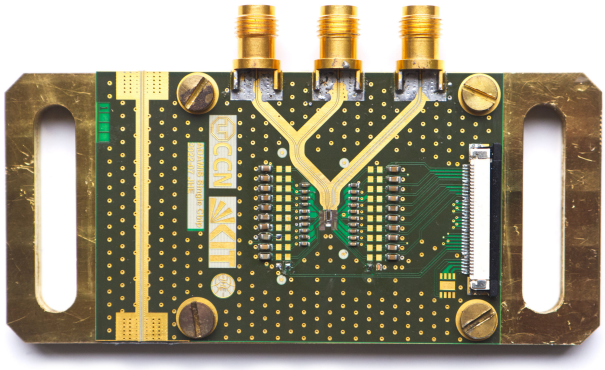

Fig. 7. Overview of the designed PCB with edge-mount connectors for supplying the LO and differential BB signals.

A printed circuit board (PCB), shown in Fig. 7, was designed to allow the characterization in the laboratory. A flexible flat ribbon cable is used to supply the DC voltages reducing physical strain on the assembly. With the IC placed in a cavity, electromagnetically modeled transmission lines feed the single-ended LO signal and the differential BB signal. All chip-to-board connections are made via wire bonding. GSG and GSSG interfaces were used with optimized geometries on the PCB side to reduce attenuation and improve the matching by minimizing the necessary bond wire lengths. High-frequency edge-mount connectors allow the connection of $1.85\,\text{mm}$ cables to attach laboratory signal sources and bit pattern generators. The RF output is probed for all following measurements.

A. Analysis of the Small-Signal Behavior

The measurement setup used to determine the small-signal behavior is depicted in Fig. 8. For the inputs, a $67\,\text{GHz}$ vector network analyzer was calibrated with a $1.85\,\text{mm}$ calibration kit connected at the end of the used coaxial cables. While characterizing one PCB input, the other terminals were terminated to $50\,\Omega$. Both the LO and BB inputs were measured at the side-mount connector, including the RF transmission lines on the PCB. The output was characterized while input signals were supplied. Frequency converter modules are used to extend the frequency spectrum to a band from $220\,\text{GHz}$ to

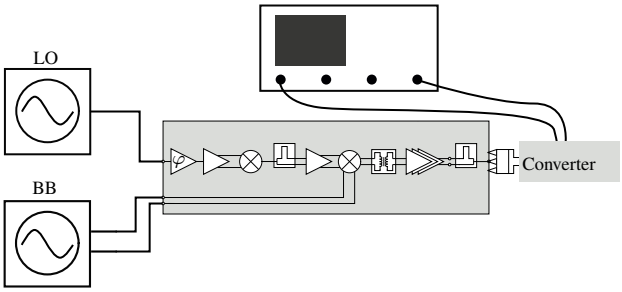

Fig. 8. Small signal measurement setup for the output characterization using a frequency extension module in the 220 GHz to 330 GHz band.

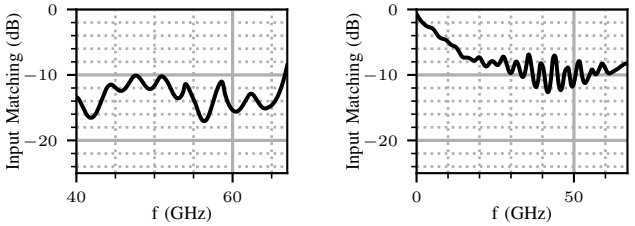

Fig. 9. Measured reflection behavior at the (a) LO and (b) BB inputs from from 40 GHz to 67 GHz and from 0 GHz to 67 GHz respectively.

330 GHz. A substrate with a variety of standards is used for calibration, establishing the reference plane at the probe tip.

The LO port, as shown in Fig. 9(a), matches better than $-10\,\mathrm{dB}$ around the center frequency of $61.5\,\mathrm{GHz}$. While the BB inputs were separately measured, the mixed-mode S-parameters were calculated post-measurement [26]. The differential-differential reflection is depicted in Fig. 9(b). A match of better than $-9\,\mathrm{dB}$ is achieved for frequencies higher than $20\,\mathrm{GHz}$, which matches the expected circuit characteristics. The RF output matching behavior, shown in Fig. 10, was measured at the on-chip GSG pad at the output of the passive balun. A reflection factor of less than $-4\,\mathrm{dB}$ is achieved over the frequency range from 220 GHz to 330 GHz. The simulated resonances at 245 GHz and 275 GHz are shifted to 235 GHz and 290 GHz respectively, which can be attributed to the uncertainties in the bondwire interface. The deviations between simulation and measurement results are limited and normal operation can be expected.

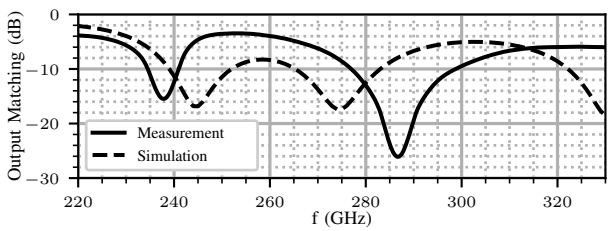

Fig. 10. Measured and simulated reflection behavior at the RF output from 220 GHz to 330 GHz.

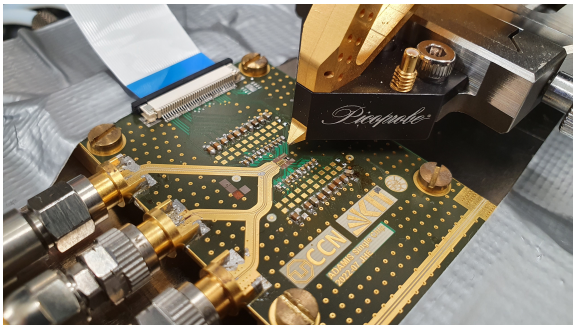

Fig. 11. Close-up of the RF PCB feeding the DC and RF signals mounted on the wafer prober.

B. Analysis of the Large-Signal Behavior

The large-signal behavior was characterized using two separate laboratory signal sources feeding the LO and BB inputs. At the BB port, an external balun creates the differential signal. Both input signals were power calibrated at the reference plane of the edge-mount connectors for every power and frequency step, compensating for any cable or connector losses, thereby producing constant input power values over the respective operating conditions. The system is characterized up to a BB input frequency of $26\,\mathrm{GHz}$ resulting in a RF bandwidth of $52\,\mathrm{GHz}$ and a measured output band ranging from 220 GHz to 272 GHz. At the output, an external broadband waveguide-to-coaxial down-conversion mixer (WR3.4MixAMC-I by Virginia Diodes) capable of operating in the spectrum from 220 GHz to 330 GHz with $40\,\mathrm{GHz}$ of IF bandwidth is attached to the probe. The necessary LO signal for this mixer ($\mathrm{LO_{mix}}$) is supplied by a third signal source, which is tightly coupled to the LO source of the device under test (DUT). The measurement script controls $\mathrm{LO_{mix}}$ to achieve a low-IF down-conversion with a $240\,\mathrm{MHz}$ frequency offset, alleviating the need for a coherent reception and enabling the characterization of the LO feedthrough and RF power. Finally, a frequency spectrum analyzer attached to the IF output of the broadband mixer evaluates the corresponding frequency components up to 67 GHz. Fig. 11 shows the measurement assembly mounted on the wafer prober.

The RF spectrum centered around the fixed LO frequency of $246\,\mathrm{GHz}$ of the double-sided output power at a constant LO power level of $-10\,\mathrm{dBm}$ and $-5\,\mathrm{dBm}$ of constant BB power is depicted over the RF bandwidth in Fig. 12. The RF bandwidth BW_{RF} calculates as the difference between the two output tones $BW_{\mathrm{RF}} = 2 \cdot f_{\mathrm{BB}}$. A quadratic fit of the measurement data is given as a dashed gray line to ease the analysis and allow for precise bandwidth evaluation. Simulations and measurements fit together within a deviation of less than $4\,\mathrm{dB}$ towards the end of the spectrum. The most likely explanation for this deviation between simulation and measurement is a load estimation misalignment introduced by uncertainties produced by the manual bondwire interface and probing at the output of the power amplifier. A maximum output power of $3.5\,\mathrm{dBm}$ is achieved at $2\,\mathrm{GHz}$ of bandwidth with a 3-dB bandwidth of $26.15\,\mathrm{GHz}$. The simulation predicts the LO feedthrough

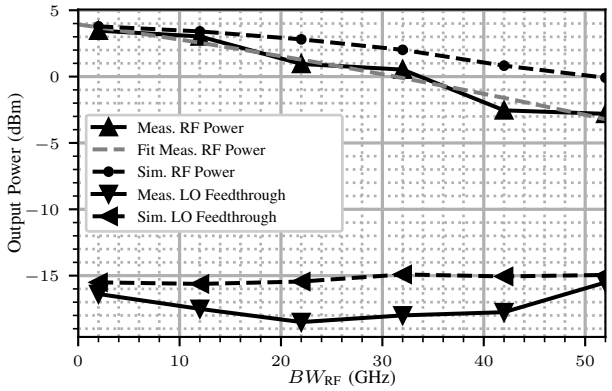

Fig. 12. Measured and simulated high frequency double-sideband power spectrum and LO feedthrough power over total RF bandwidth BW_{RF} centered around the 246 GHz LO signal. The analyzed spectrum ranges from from 220 GHz to 272 GHz. At the PCB ports, $-10\,\mathrm{dBm}$ of LO power and $-5\,\mathrm{dBm}$ of BB power are supplied. A quadratic fit of the RF output power is given in dashed gray. Simulated results for both the RF and LO values are given as black dashed lines.

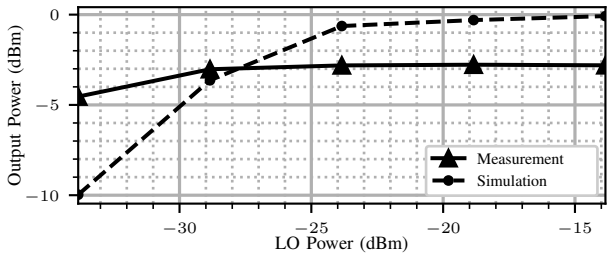

Fig. 13. Measured and simulated LO power sweep with the output tones at $246 \pm 26\,\mathrm{GHz}$ and $-5\,\mathrm{dBm}$ at the BB port.

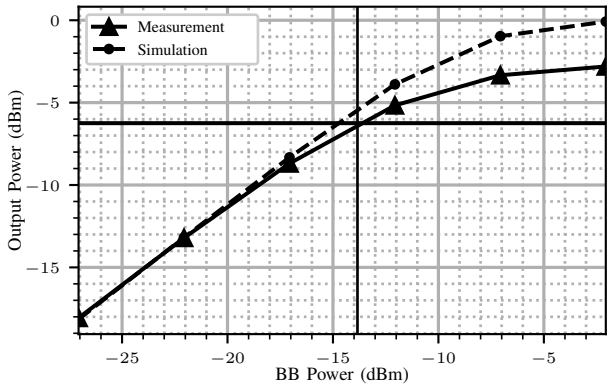

Fig. 14. Measured and simulated double-sideband output power for a a BB input power sweep with the output tones at $246 \pm 26\,\mathrm{GHz}$ of RF bandwidth and $-10\,\mathrm{dBm}$ at the LO port.

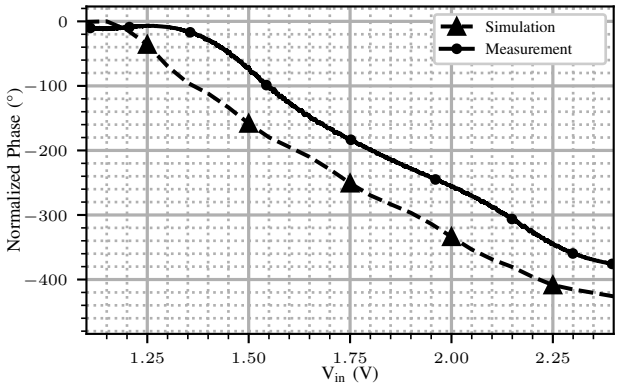

Fig. 15. Measured and simulated results of the phase steering behavior at 246 GHz over the tuning voltage range of 1 V to 2.5 V.

and generally remains at power levels of less than $-17\,\mathrm{dBm}$, which results in a LO suppression of 12 dB in the worst case at the highest characterized bandwidth.

A LO power sweep is given in Fig. 13 at the maximum RF bandwidth of 52 GHz and a BB input power of $-5\,\mathrm{dBm}$. The simulation predicts the measurement results well while experiencing the a drop in power by less than 4 dB confirming the behavior shown in Fig. 12. The PCB losses were de-embedded according to a reference thru-line measurement to allow for precise system characterization. At LO power levels higher than $-29\,\mathrm{dBm}$, the LO chain produces enough power to achieve saturation of the mixer.

The BB power was swept at a LO input power of $-10\,\mathrm{dBm}$ and the maximum bandwidth of 52 GHz, as shown in Fig. 14. The simulation and measurement results match for low BB power values with a comparably earlier output power compression of the measured DUT. At the input referred 1-dB compression point of $-15.4\,\mathrm{dBm}$, the measured $\mathrm{P_{o,1dB}}$ is $-6.25\,\mathrm{dBm}$. This results in a small-signal gain of 10.15 dB, referred to the BB power.

Characterizing the phase steering capability is challenging. Due to the frequency conversion in the LO chain a typical phase characterization using a vector network analyzer is not possible and an alternative measurement method was devised: Turning off the BB input signal produces a direct one-tone measurement of the up-converted LO signal at the output, enabling the characterization of the phase steering behavior. The spectrum analyzer is replaced with a real-time oscilloscope (RTO) that records the output signal's time-series data. A 100 kHz sine signal is used to sweep the phase tuning voltage over the entire input amplitude from 1 V to 2.5 V. In the following, the obtained phase-modulated signal is discretized for two periods of the control signal and decoded with a software IQ-receiver reconstructing the phase information. The necessary reference signal is determined by fitting a sine with the LO frequency and constant phase to the first four signal periods, which is possible as the frequency of the output signal of the harmonic mixer at 240 MHz is much higher than the phase modulation frequency. The resulting phase measurement is given in Fig. 15. Both simulation and measurement show the expected linear relation with the input voltage [10] and move in parallel within an offset in the absolute phase. Beam control is possible with a phase range of approximately 380°. The deviation from the usual 360° is due to the I and Q path of the phase shifter being slightly off quadrature. In practice, the reference phase setting is in the center of the phase tuning range. More than 360° of phase range enables the use of the most linear section of the characteristic in terms of phase versus tuning voltage, resulting in a simplified steering algorithm based on a linear fit on the

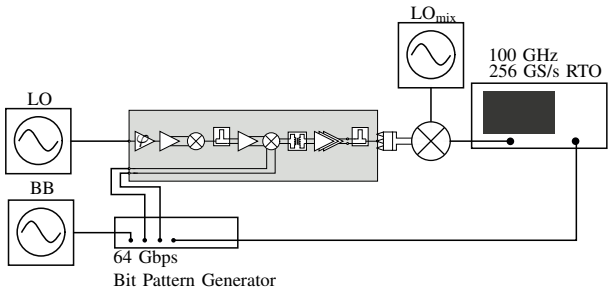

Fig. 16. Measurement setup for the bit pattern characterization.

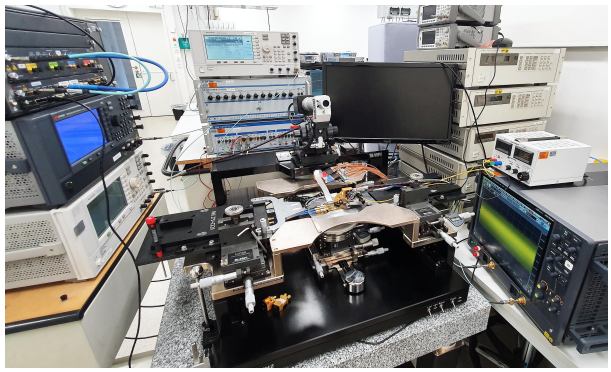

Fig. 17. Photograph of the measurement setup used to characterize the data transmission performance in the laboratory.

measurement data while enabling high-precision phase control.

C. Analysis of the Data Transmission Behavior

The receiver chain for the data reception consists of a wideband down-conversion mixer, probing the RF output, and a high-speed RTO, as depicted in Fig. 16. By avoiding the use of an antenna, the uncertainty in the transmitter characterization is reduced. First, the signal is down-modulated to an intermediate frequency to preserve the complex signal information and is sampled at $256\,\mathrm{GS/s}$ in $20\,\mu\mathrm{s}$ time frames. The transmitted signal from the data source is split and fed to a second channel of the oscilloscope as a reference signal to enable the bit error rate (BER) calculation. A photograph of the measurement setup in the research laboratory is shown in Fig. 17. The fabricated IC is tested for data rates ranging from $16\,\mathrm{Gbps}$ to $60\,\mathrm{Gbps}$.

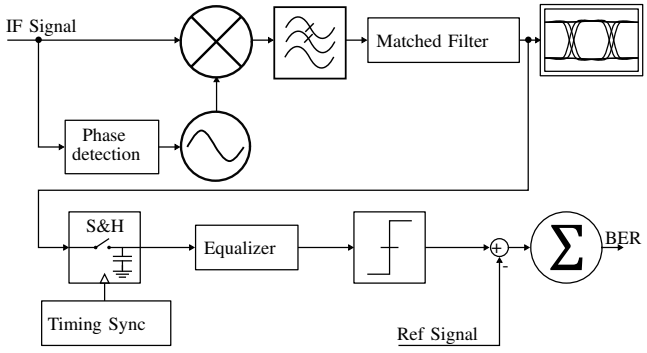

Fig. 18. Simplified overview of the architecture of the designed software defined receiver.

Previously shown systems characterize transmitters and receivers together due to the unavailability of suitable broadband measurement equipment, leading to remaining uncertainties about the behavior of the individual circuit blocks. This work employs commercially available equipment, like the WR3.4MixAMC-I by Virginia Diodes, to measure the transmitter. However, the presented transmitter circuit exceeds the IF bandwidth of obtainable broadband receivers. Without full IQ demodulation available, the sampling rate of the RTO further reduces the maximum recordable data rate. The resulting effects are discussed below: The precise demodulation of large bandwidth signals post-measurement in software poses severe challenges. $\mathrm{LO_{mix}}$ feedthrough and regeneration in the IF signal adds coherent noise that necessitates carefully placed filters to limit the degradation of the signal-to-noise ratio (SNR). Filtering unwanted signal components is another hurdle, as the signal already covers most of the available baseband spectrum. Especially for the higher data rates, self-interference of the sidebands is a limiting issue that necessitates a filter in the RF domain. However, filtering to the half-data rate bandwidth strips the signal of its near-constant envelope, increasing the EVM and reducing eye-opening. Further, the transmitted power is spread out due to the wide bandwidths, while noise power increases with bandwidth. This is reflected in an increase in thermal noise by $5.74\,\mathrm{dB}$ from $16\,\mathrm{Gbps}$ to $60\,\mathrm{Gbps}$. Overlayed to this is the lower dynamic range of the RTO with a low effective number of bits (ENOB) of five at full bandwidth. At $160\,\mathrm{mV}$ full scale, this gives a voltage sensitivity of $5\,\mathrm{mV}$ with a manufacturer-specified RMS noise of $1.5\,\mathrm{mV}$. From the evaluated spectrum, a decrease of the SNR by $25\,\mathrm{dB}$ is visible going from $16\,\mathrm{Gbps}$ to $60\,\mathrm{Gbps}$. Lastly, cable frequency-dependent attenuation can reach values up to $2\,\mathrm{dB}$ around the IF frequency distorting the signal.

The received signal is processed in the digital domain with the receiver architecture shown in Fig. 18. The phase is extracted from the carrier leakage and used to compensate for drift between the different signal sources within a sampled time frame. Next, the down-modulated signal is filtered by a data rate adaptive matched filter with a beta of 0.35. From this signal, the bit-timing is synchronized, and the samples are taken.

The reference signal is aligned to the received signal for the BER measurement to compensate for path-length delay differences in the measurement setup by correlating the signals. A 65-tap equalizer is realized in software and compensates for the channel effects caused by the measurement equipment. The equalized signal is compared to the received sequence post-measurement, and the bit errors and the total number of bits are counted for the BER measurement. Automating the measurement and processing allows for repeating the process until enough bits are sampled to reach the desired confidence level of $95\,\%$ for BER down to $5 \cdot 10^{-8}$.

Fig. 19 shows the resulting eye diagrams for different data rates from $16\,\mathrm{Gbps}$ to $56\,\mathrm{Gbps}$. The achievable data rate

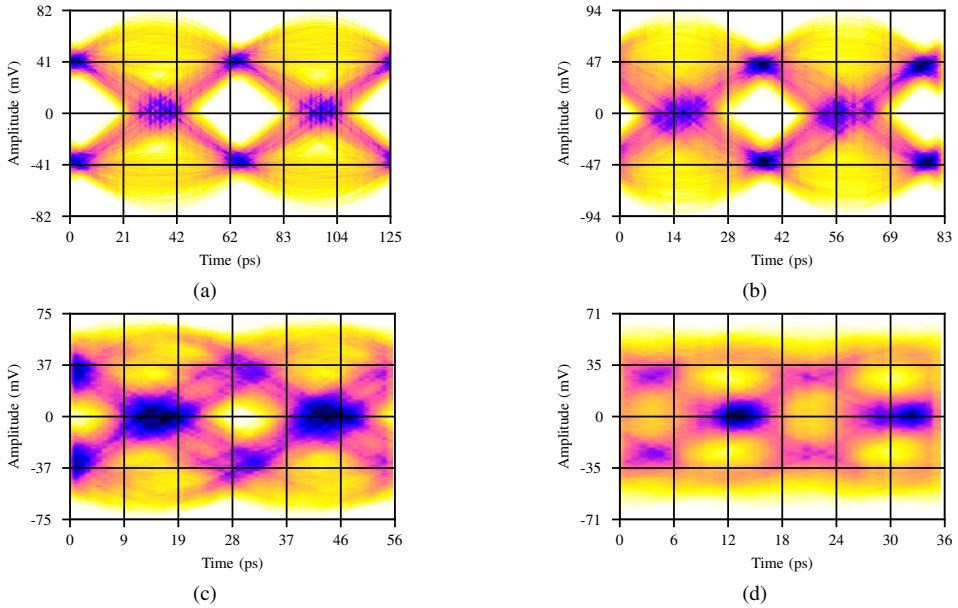

Fig. 19. Measured eye diagrams for an input amplitude of V_{pp}=200 mV. (a) 16 Gbps. (b) 24 Gbps. (c) 36 Gbps. (d) 56 Gbps.

TABLE I
OVERVIEW OF STATE-OF-THE-ART MILLIMETER WAVE TRANSMITTERS IN SILICON TECHNOLOGIES OPERATING AT AROUND 200 GHZ

	This Work	**[3]**	**[27]**	**[28]**	**[4]**	**[5]**	**[1]**
Technology	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	65 nm CMOS
Modulation	BPSK	BPSK	BPSK/ QPSK	QPSK	BPSK	16-QAM	OOK
Transmitter modules	360° LO-Phase Steering, LO×4, LO Buffer, Modulator, PA	BB Buffer, LO×8, LO Buffer, Modulator, PA	LO×16, LO Buffer, IQ-Modulator, PA	LO×16, LO Buffer, IQ-Modulator, PA	LO Buffer, Mixer	LO×16, LO-Buffer, IQ-Modulator, BB-Buffer, PA	Hybrid, LO-Buffer, RF-Switch, PA, LO×4
Center frequency (GHz)	246	240	240	230	190	230	260
3 dB bandwidth (GHz)	26.15	35	20	35	60	28	—
$P_{RF,TX}$ (dBm)	3.5	-0.8	-4.4	4.5*	-6	5	-3
iP1dB (dBm)	-15.4	-25	-15	—	-7	-14	—
Data rate (Gbps)	52	25	25	65	40/ 50	100	10
P_{DC} (mW)	414	625*	1033	960	32	960	688
η_{RF}† (%)	0.54	0.13	0.04	0.29	0.78	0.33	0.07
Transmitter efficiency (pJ/bit)	8.0	25.0	41.3	14.8	3.9/ 3.1	9.6	68.8
Area (mm^2)	1.16	1.25	1.61	1.40	0.70	1.52	3.00

†: $\eta_{RF} = P_{RF,TX}/P_{DC}$; *: estimated

is conservatively determined at 52 Gbps supported by the characterized large-signal spectrum. With the system power consumption of 414 mW, a maximum transmitter efficiency of 8.0 pJ/bit is achieved at 52 Gbps. With data rates tested up to 60 Gbps, the resulting eye diagrams and BER leads to the conclusion, that the available measurement equipment is limiting the evaluation of the full potential chip.

The results for data rates up to 60 Gbps are depicted in Fig. 20. It becomes evident that the BER increases quite significantly over 30 Gbps and reaches a values of higher than 10^{-3} above 40 Gbps. Further analysis of the receiving system shows that this increase results from the receive mixer topology with a diode, spurious tones from the multiplier chain also visible in the IF spectrum, and self-interfering with the received signal. The theoretical analysis of this receiving setup with an ideal and error-free transmit signal is also shown in Fig. 20. It matches the actual achieved BER leading to the conclusion that the transmitter is better than the receiving system. The simulation assumes a square law relation in the mixing diode and harmonics above and below the actual LO tone with power levels corresponding to IF and RF measurements of the receiver.

V. CONCLUSION

This research article presented a fully integrated broadband BPSK transmitter with LO phase steering capability and a compact power amplifier achieving data rates up to 52 Gbps. The fabricated IC was studied and characterized in the research laboratory. While many designs employ complex modulation schemes to achieve high data rates in a narrow band channel, this work exploits the large available bandwidth around 246 GHz. It was shown that broadband designs featuring

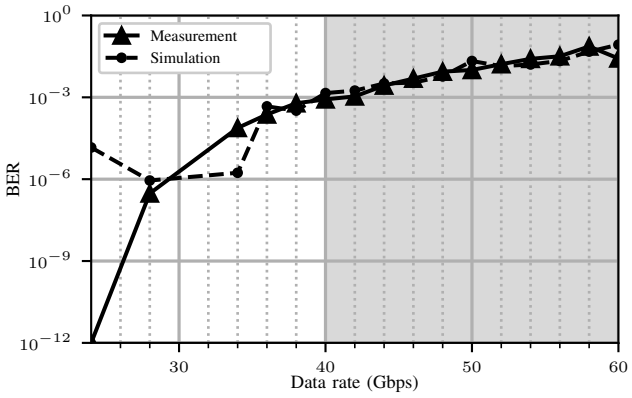

Fig. 20. Measured bit error rate over data rates up to 60 Gbps. The gray background marks the section of the analysis were the signal bandwidth exceeds the IF bandwidth of the laboratory receiver leading to a strong influence on the error performance.

low-order modulation schemes can compete with more involved architectures in terms of data rate while reducing the overall power consumption significantly, resulting in very high efficiency. The design extends the transmitter functionality by incorporating LO phase control in the LO frequency multiplication-by-4 signal chain. This significantly reduces the LO generation and distribution complexity and enables the combination of multiple transmitters in a dynamically steerable phased array. An overview of transmitter designs operating at similar frequencies is given in Tab. I. Data rates up to $52\,\mathrm{Gbps}$ have been demonstrated, which is the highest reported result for BPSK systems, and the respective bit-error rates are calculated. Here, the transmitter outperformed the available measurement equipment. While some designs, based on BPSK modulation, have shown data rates approaching the presented design [4], this is the first complete transmitter with LO multiplying signal chain and power amplifier achieving these data rates. The presented transmitter produces a high saturated RF output power of $3.5\,\mathrm{dBm}$ while consuming $414\,\mathrm{mW}$. The achieved RF efficiency of $0.54\,\%$ is twice as high as the closest competitor [28]. At a transmitter efficiency of $8.0\,\mathrm{pJ\,bit^{-1}}$ this circuit consumes $32\,\%$ of the energy per bit compared to BPSK realizations [3], [27] and $54\,\%$ compared to QPSK architectures in the same frequency band [28]. At less than half the power consumption, the efficiency is improved by $17\,\%$ in comparison to higher order 16-QAM systems [5], even without including the additional power consumption of the necessary, more elaborate BB chains.

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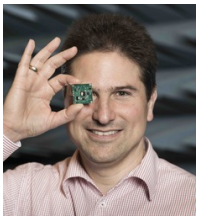
BIOGRAPHY

Luca Steinweg was born in Bad Säckingen, Germany, in 1994. He received the Dipl.-Ing. degree in electrical engineering from Technische Universität Dresden, Germany, in 2019. His diploma thesis was done in co-operation with Rohde & Schwarz GmbH & Co. KG in Berlin where he investigated broadband power detectors. He is currently pursuing the Ph.D. degree at the Chair for Circuit Design and Network Theory at Technische Universität Dresden. His research focus lies in millimeter-wave wireless transmitters in BiCMOS technology.

Joachim Hebeler was born in Homberg (Efze) in 1994. He received his B.Sc. degree in electrical engineering from the University of Kassel, Germany in 2016 and his M.Sc. in electrical engineering from the University of Kassel, Germany in 2018. He is currently pursuing his Ph.D. at the Institute of Radio Frequency Engineering and Electronics (IHE) in Karlsruhe. His research focus are mm-wave integrated circuits, especially power amplifier systems in SiGe, as well as packaging and antenna solutions in the sub-terahertz regime.

Tilo Meister received the Diploma degree in electrical engineering and the Ph.D. (Dr.-Ing.) degree from the Technische Universität Dresden, Dresden, Germany, in 2006 and 2012, respectively. He is currently a Senior Researcher and the FFlexCom Program Manager with the Chair for Circuit Design and Network Theory, Technische Universität Dresden. His research interests include modeling and circuit design for flexible electronics, Beyond Moore's technologies, and millimeter-wave IC design in silicon-based technologies.



Thomas Zwick received the Dipl.-Ing. (M.S.E.E.) and the Dr.-Ing. (Ph.D.E.E.) degree in electrical engineering from the Universität Karlsruhe (TH), Karlsruhe, Germany, in 1994 and 1999, respectively. From 1994 to 2001, he was a Research Assistant with the Institut für Hochstfrequenztechnik und Elektronik (IHE), TH. In February 2001, he joined IBM as a Research Staff Member with the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA. From October 2004 to September 2007, he was with Siemens AG, Lindau, Germany, where he managed the RF development team for automotive radars. In October 2007, he became a Full Professor with the Karlsruhe Institute of Technology, Karlsruhe, Germany. He is the Director of the IHE, TH. He has co-edited three books, authored or coauthored 120 journal papers, over 400 contributions at international conferences, and 15 granted patents. His research interests include wave propagation, stochastic channel modeling, channel measurement techniques, material measurements, microwave techniques, millimeter wave antenna design, wireless communication, and radar system design.

Frank Ellinger was born in Friedrichshafen, Germany. In electrical engineering (EE), he graduated in 1996 from the University of Ulm, Germany. He received a diploma degree in business and administration, and a doctor degree in EE from the ETH Zürich, Switzerland, in 2001. For his habilitation thesis he obtained the venia legendi (university teaching degree) in high frequency circuit design from the ETH in 2004. In this area, Mr. Ellinger has been lecturer at the ETH between 2002 and 2006. From 2001-2006, he has been head of the RFIC Design Group of the Electronics Laboratory at the ETH, and project leader of the IBM/ETH Competence Center for Advanced Silicon Electronics at IBM Research in Rüschlikon. Since August 2006, he is full professor and head of the Chair for Circuit Design and Network Theory at the Technische Universität Dresden, Germany. His core expertise is in the area of integrated circuits for wireless and optical communications. Prof. Ellinger is the coordinator of the BMBF zwanzig20 cluster FAST (Fast Actuators Sensors and Transceivers) with 90 partners and the speaker of the DFG priority program FFlexCom. He was the coordinator of the communication systems area of the BMBF cluster Cool Silicon and member of the management board of the Cool Silicon e.V. Prof. Ellinger is/was the coordinator of several EU funded projects, e.g. DIMENSION, ADDAPT, RESOLUTION, MIMAX und FLEXIBILITY. In the period between 2005 and 2006, he served as associated editor for the IEEE Microwave and Wireless Component Letters. He was organizer and chair of several conferences, e.g. the European Solid State Circuits Conference (ESSCIRC) 2018. He published more than 500 refereed scientific papers. Frank Ellinger has been elected by the IEEE Microwave Theory and Techniques (MTT) Society as IEEE Distinguished Microwave Lecturer. For his works, he received several awards including the Vodafone Innovation Award, the Alcatel Lucent Science Award, the IEEE MTT-S Outstanding Young Engineer Award, the ETH Medal, the Denzler Award of the Swiss Federal Association of Electrical Engineers, twice the Rohde & Schwarz, Agilent and Gerotron EEEfCOM Innovation Award.