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Monolithic Integration, Performance and Comparison of Self-Aligned and Conventional IGZO Thin-Film Transistors on a Flexible Substrate

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***Abstract*—Flexible electronics, most prominently thin-film transistors (TFTs) on plastic substrates are considered the prime building block for the realization of innovative wearable systems. Two of the currently most successful fabrication processes of transistors on free standing polymer foils are large-area compatible devices structured by conventional UV lithography and high-speed transistors realized by self-alignment. Here, both processes, based on InGaZnO technology, are combined for the first time. This demonstrates their compatibility, but also showcases the differences between the resulting devices. Concerning the geometry, TFTs with the same nominal designed channel length of $1.5\,\mu m$, exhibit real channel length of $1.5\,\mu m$ (self-aligned) and $4.5\,\mu m$ (conventional). Furthermore, the integrated side by side fabrication enables the electrical comparison of both types of TFTs excluding external factors. While all TFTs exhibit similar threshold voltages around $0\,V$ and excellent on/off ratios of $\approx 10^{10}$, conventional TFTs are easier to fabricate, and have comparably higher mobilities up to $16\,cm^2\,V^{-1}\,s^{-1}$. At the same time, self-aligned TFTs demonstrate better AC performance, demonstrating a maximum oscillation frequency of $216\,MHz$. This integration shows new possibilities for the realization of complex systems made from building blocks optimized for reliability and speed.**

***Index Terms*—Flexible electronics, Self-alignment, InGaZnO, Thin-Film Transistors, AC performance**

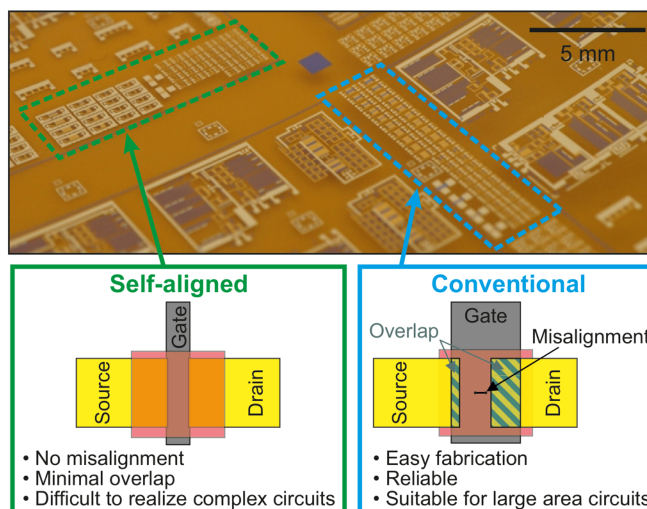

Fig. 1. Integration: Self-aligned and conventional non-self aligned TFTs realized on a single polyimide substrate using an integrated fabrication process.

I. Introduction

FLEXIBLE thin-film electronics on large-area plastic substrates have the potential to unobtrusively integrate electronic functionality into everyday objects and hence to connect physical objects to the digital domain [1]. In this context, novel technologies and materials for the fabrication of electronic devices on flexible, but mostly fragile substrates are being developed. Among various types of amorphous and (poly-)crystalline Silicon thin-films, organic semiconductors, carbon nanotubes and different two dimensional materials [2]–[6], oxide semiconductors, in particular amorphous InGaZnO (IGZO) [7], are suitable materials for the realization of thin-film transistors (TFTs). This is because IGZO provides a good compromise between large area and low temperature fabrication compatibility as well as electrical and mechanical performance. This is reflected by the recent demonstration of complex digital circuits as well as analog systems [8], [9]. Although, the realization of circuits on flexible free-standing large-area substrates which are fast and complex at the same time remains a significant challenge, recent advances resulted in very fast flexible TFTs. Highly scaled flexible InSnO (ITO) and silicon based devices with channel length down to $160\,nm$ exhibited transit frequencies of $2.1\,GHz$ and $3.7\,GHz$ have been reported [10], [11]. However, these are normally fabricated using electron beam lithography, or

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the transfer of crystalline semiconductor membranes which is not easily scalable and also not compatible with large-area substrates. Other techniques to realize miniaturized TFTs on flexible substrates include focused ion beam milling [12], and two photon laser writing [13], which are also sequential and therefore not easily scalable processes. An alternative process is the fabrication of self-aligned TFTs using e.g. backside illumination. Such processes are regularly employed for oxide based TFTs and resulted in IGZO and ZnO TFTs with transit frequencies (f_T) of 1.1 GHz or maximum oscillation frequency of 2.7 GHz, respectively [14], [15]. On a flexible substrate, such a process resulted in flexible IGZO TFTs with a transit frequency f_T of 135 MHz, and a maximum oscillation frequency f_{MAX} of 0.4 GHz [16], [17]. By combining this advanced fabrication techniques with conventional fabrication protocols, the advantages of both processes can open up a pathway to more complex, but still fast flexible circuits. As indicated in Fig. 1, this report presents the integration of both conventional and self-aligned TFTs on the same flexible substrate. This not only demonstrates the compatibility of the two technologies, but also allows a direct and absolute fair comparison of the performance of the resulting transistors. The individual features of the two realized types of transistors are described below.

A. Conventional TFTs

Conventional TFTs, i.e. transistors entirely fabricated by standard UV lithography, etching and liftoff processes can be fabricated on flexible substrates since decades [18]. Compared to other flexible TFTs, such devices are easy to fabricate, highly reliable, and reproducible, proven by the demonstration of circuits with thousands of TFTs [19]. At the same time, their minimum channel length is particularly limited if conventional TFTs are fabricated on a free standing substrate. Additionally, tolerances are needed to compensate for the expansion and shrinkage of the substrate during the fabrication process. Changes of the substrate size are caused by thermal expansion as well as swelling due to the absorption of liquids. These size variations can reach values of $>10\,\mu m$ on a centimeter sized substrate [16], resulting in misalignment and the need for overlaps between the gate and source-drain metal as shown in Fig. 1-bottom right. This in turn leads to unwanted parasitic capacitances making the realization of fast flexible TFTs by conventional lithography difficult.

B. Self-aligned TFTs

Flexible TFTs with self-aligned source and drain contacts benefit from the fact that a misalignment of the channel is inherently excluded, and overlaps are minimized. This is because the gate materialization itself acts as mask to structure the TFT channel. This is a significant advantage for the fabrication on flexible substrates, and also eliminates the need for dedicated gate to source/drain overlaps which in turn reduces the parasitic capacitance of the gate. Furthermore, this approach normally simplifies the fabrication of very short TFTs, which makes this technique ideal for high speed devices (illustrated in Fig. 1-bottom left). The shortest flexible TFTs so far realized with the technique used here exhibit a channel length of $0.5\,\mu m$ [16]. At the same time, self-aligned TFTs require additional process steps, which can limit the choice of usable materials. e.g. the gate contacts must be resistant against the source drain materialization etching solution. More importantly, self-aligned TFTs require transparent substrates. Unfortunately the transparency of high temperature compatible polymer superstates is often limited. If only partially transparent substrates are used, the uniformity of the self-alignment process can be reduced (mostly due to the absorption of light and the associated heating of the substrate), affecting the reliability of self-aligned TFTs on large areas.

II. Device manufacturing

All TFTs were directly fabricated on a free-standing $7.4\,cm \times 7.4\,cm$ large polyimide foil using vacuum deposition processes, standard UV lithography and self-aligned lithography. An overview of the fabrication process is given in Fig. 2aI. The maximum temperature employed during the fabrication process was $150\,^{\circ}C$.

A. Device structure and materials

A bottom-gate inverted staggered and passivated device structure was used to realize all TFTs. The device stack includes Ti gates. This choice of gate material ensures good adhesion to the substrate and resistance against the etching solutions used during the fabrication process. SiN_x is used as barrier layer, while Al_2O_3 is used as dielectric because it provides a large relative permittivity of ≈9.5, and forms a high quality interface with the IGZO semiconductor. Finally, Cr and Ti are used as adhesion layers while Au is utilized for the contacts.

All devices were fabricated on a free-standing $50\,\mu m$ thick polyimide foil (Kapton E). This material provides a large elastic modulus of $\approx 5\,GPa$ [20] and is partially transparent (the measured transmittance is shown in Fig. 2aII). While there are alternative and more transparent polymer foils available for the fabrication of thin-film devices [21]–[23], polyimide is still one of the most common substrates [24]. This is due to its thermal and chemical stability, exhibiting a coefficient of thermal expansion of $12\times10^{-6}\,K^{-1}$, and a humidity expansion coefficient of $9 \times 10^{-6}\,\%RH^{-1}$ [25].

To make the self-aligned and conventional TFT technologies as comparable as possible, the two types of TFTs were designed with the same dimensions on the lithography masks. Long channel devices with a channel width of $50\,\mu m$ and a channel length of $10\,\mu m$, and short channel devices with a channel width of $50\,\mu m$ and a channel length of $1.5\,\mu m$ were fabricated. Here, the channel length of the conventional TFTs is defined by the distance between the source and drain contacts, while for self aligned TFTs the channel length is defined by the length of the gate contact. In addition, conventional TFTs exhibit gate to source/drain overlaps of $15\,\mu m$ (long channel), and $5\,\mu m$ (short channel) on the mask. The corresponding high-resolution photo masks were purchased from Computergarphics Jena. The pad layout of the TFTs uses a GSG geometry with a pitch of $150\,\mu m$ (Fig. 2b). This enables reliable AC characterization through GSG probe tips.

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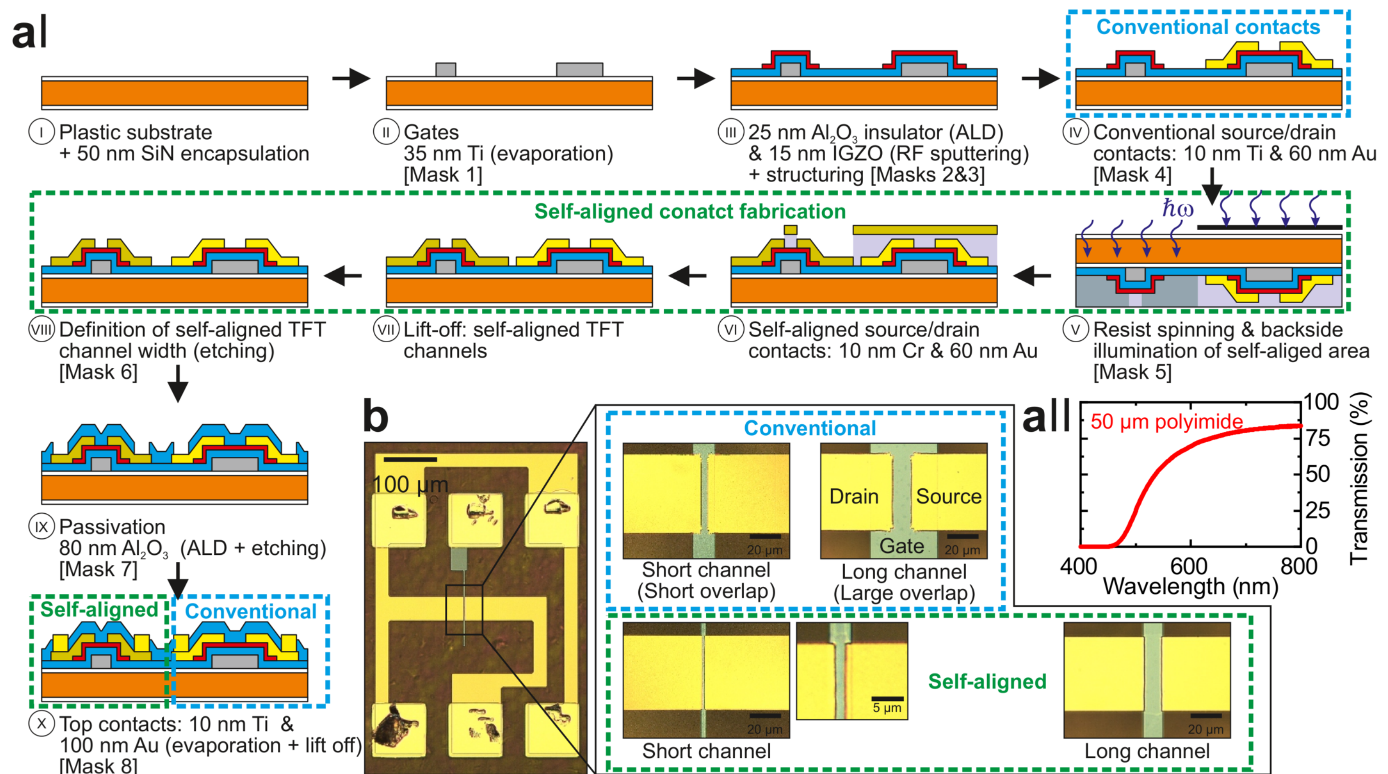

Fig. 2. Fabrication: aI) Schematic of the fabrication process flow for the realization of monolithically integrated conventional and self-aligned TFTs on a flexible $50\,\mu\mathrm{m}$ thick polyimide foil. aII) Measured transmission spectrum of the polyimide foil used as substrate. b) Micrograph of representative long and short channel TFTs, from the same substrate, fabricated using self-aligned and conventional lithography.

B. Fabrication

First, the polyimide substrate was cleaned with acetone and isopropanol in an ultrasonic-bath, and then stored in an oven at $200\,^{\circ}\mathrm{C}$ for $24\,\mathrm{h}$. Next, both sides of the substrate were covered with $50\,\mathrm{nm}$ thick SiN_x using a plasma-enhanced chemical vapor deposition process at $150\,^{\circ}\mathrm{C}$ (Oxford Instruments PECVD 80+). The initial step of the TFT fabrication process itself was the e-beam evaporation of a $35\,\mathrm{nm}$ thick Ti bottom gate (Plassys). This layer was structured via lift-off [UV lithography: mask 1]. The gates were insulated by $25\,\mathrm{nm}$ thick Al_2O_3 grown by atomic layer deposition (ALD) at $150\,^{\circ}\mathrm{C}$ using water and trimethylaluminium as precursors (Picosun Sunale R-150B). Next, $15\,\mathrm{nm}$ thick IGZO was deposited at room temperature using RF magnetron sputtering, a ceramic target with an atomic composition of In:Ga:Zn:O = 1:1:1:4, and a pure Ar atmosphere (PVD systems). Both the IGZO layer and the Al_2O_3 layer were structured by wet chemistry, using HCl:H_2O = 1:120 , and HNO_3: H_3PO_4: CH_3COOH: H_2O =1:25:5:5, respectively [UV lithography: masks 2+3].

To realize the source and drain contacts on the conventional TFTs, $10\,\mathrm{nm}$ of Ti, and $60\,\mathrm{nm}$ Au were e-beam evaporated (Plassys), and structured by lift-off [UV lithography: mask 4].

The realization of self-aligned source and drain contacts started with the deposition of positive AZ 4533 photoresist. The areas of the substrate carrying self-aligned TFTs were then illuminated through the backside of the partially transparent substrate using the opaque Ti gates as mask. This was done using a LOT Oriel Hg UV lamp at $400\,\mathrm{W}$. The optical power transmitted through the polyimide substrate (measured at a wavelength of $400\,\mathrm{nm}$) is $0.04\,\mathrm{mW\,cm^{-2}}$. To account for this, the total exposure time was $16\,\mathrm{min}$. Here, a metallic mask [masks 5] was used to shield the conventional TFTs. An additional conventional lithography can be used to illuminate the photoresist on top of the gate contact pads of self-aligned transistors [UV lithography: mask 5a]. This step was performed to demonstrate its feasibility, but is not relevant for the fabrication of individual devices, however, it is essential if circuits should be realized. The resist was developed for $225\,\mathrm{s}$ using AZ developer. This development time removed virtually all exposed resists. At the same time, it also determines the final gate to source/drain overlaps due to the unavoidable over-development of the positive photo-resists. After the resist development, a line of photo resist was perfectly aligned to each gate. To form the TFT channels, $10\,\mathrm{nm}$ of Cr and $60\,\mathrm{nm}$ of Au were e-beam evaporated (Plassys) and structured by lift-off using the self-aligned resist. Finally, the channel width and the contact pads of the self-aligned transistors were defined by wet etching using $50\,\mathrm{g}$ $(NH_4)_2Ce(NO_3)_6$ + $12\,\mathrm{g}$ CH_3COOH + $250\,\mathrm{mL}$ H_2O and $15\,\mathrm{g}$ KI + $5\,\mathrm{g}$ I + $100\,\mathrm{mL}$ H_2O to etch the Cr and Au, respectively [UV lithography: mask 6].

Subsequently, all devices on the substrate were passivated with a structured $80\,\mathrm{nm}$ thick Al_2O_3 layer, similar to the gate insulator layer [UV lithography: mask 7]. Lastly, the fabrication process was concluded by the deposition of additional contact pads made from $10\,\mathrm{nm}$ Ti (e-beam, MBRAUN EB M-4) and $100\,\mathrm{nm}$ Au (thermal, MBRAUN Evaporator ECOVap and ProVap - TP700), and structured by lift-off [UV

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lithography: mask 8].

III. Results and Discussion

The fabricated TFTs were characterized for their AC and DC performance. All measurements were carried out at room temperature under standard lab conditions. All performance parameters were extracted from TFTs in the saturation regime. Finally, to guarantee comparability, the same bias voltages were used for self-aligned and conventional TFTs.

This report focuses on the electrical performance of the fabricated TFTs. At the same time, it is worth mentioning that for flexible TFTs, the mechanical properties are also of paramount importance. However, the influence of bending on the AC and DC performance of conventional and self-aligned TFTs has been investigated in detail by our group in the past [16], [26]. There is no indication that the integration of both types of TFTs has any influence on their flexibility.

A. Geometry

A fully fabricated TFT is shown in Fig. 2b. While conventional and self-aligned, long and short channel TFTs exhibit the same dimensions on the photo masks, the micrographs show that the different source/drain fabrication techniques result in noticeably different measured channel dimensions. The channel width is increased in both cases: +$4\,\mu m$ (conventional), and +$1\,\mu m$ (self-aligned). The channel length is as designed for short channel self-aligned TFTs, and slightly increased for long channel self-aligned TFTs. At the same time, the channel length is significantly increased by values up to +$3.5\,\mu m$ for the conventional TFTs. These differences reflect the fact that the width and length of the different TFT channels are structured using different technologies (conventional lift-off, self-alignment, and etching). An overview of all TFT dimensions is given in Fig. 3a. Finally, the self aligned process results in measured short and consistent gate to source/drain overlaps of $0.8\,\mu m$.

B. DC performance & Capacitance

The DC characterization of TFTs, consisting in both voltage-current curves and capacitance-voltage curve, were performed with a Keysight B1500A parameter analyzer. The standard DC performance parameters were extracted using the Shichman-Hodges model [27] and the actual measured TFT dimensions. All TFTs were characterized in the linear and saturation regime. However, the bias voltages had to be limited when measuring the short channel TFTs to avoid a breakdown of the channel (V_{GS}<$3\,V$, V_{DS}<$2\,V$). This made it impossible to drive short channel TFTs into full current saturation for all V_{GS} values $>1\,V$ (Figs. 3cII and 3cIV). The TFT transfer and output characteristics are shown in Figs. 3b and 3c. The measurements show low gate leakage current and outstanding on/off current ratios around 10^{10}. The DC performance parameters extracted from the saturation regime are threshold voltage, effective carrier mobility, and sub-threshold swing (inverse of sub-threshold slope) as summarized in Fig. 3a. The reported values are in line with state-of-the-art flexible IGZO TFTs [24]. The most notable difference between the different TFTs concerns the effective mobility. While the intrinsic IGZO carrier mobility is the same for all devices, the effective mobility is influenced by the contact resistance. The contact resistances of these TFTs at the same time decrease with increasing gate-source voltage, and with increasing gate to source/drain overlaps (see [28] for more details). Furthermore, the contact resistance is more relevant for short channel TFTs with low channel resistance. Consequently, conventional TFTs (with larger overlap), and short channel TFTs exhibit larger effective mobilities than their corresponding counterparts. This leads to measured variations between $9.1\,cm^2\,V^{-1}\,s^{-1}$ and $16\,cm^2\,V^{-1}\,s^{-1}$. The different channel dimensions, effective mobilities and bias voltages also lead to different maximum transconductance values for long channel $0.12\,mS$ (conventional), $0.11\,mS$ (self-aligned), and short channel $0.21\,mS$ (conventional), $0.52\,mS$ (self-aligned) transistors.

The measured gate to source/drain capacitances of the TFTs are shown in Figs. 3d. These measurements were performed for different frequencies between $1\,kHz$ and $1\,MHz$ while the source and drain contacts were externally connected. For low gate bias voltages (TFT off), the measurements show the parasitic overlap capacitance, which reached values of $0.3\,pF$, $2\,pF$, and $5.2\,pF$ for TFTs with overlaps of $0.8\,\mu m$, $5.3\,\mu m$, and $16.5\,\mu m$, respectively. For positive gate bias voltages (TFT on), the measurements include both the parasitic overlap capacitance and the capacitance of the channel. The values depend on the frequency as trap states in the channel cannot be occupied and deoccupied at high frequencies [29]. The extracted total gate capacitances for long channel TFTs are $16.1\,pF$ (conventional) and $4.8\,pF$ (self-aligned), while they are only $5.3\,pF$ (conventional) and $1.45\,pF$ (self-aligned) for short channel transistors. These values correspond well with the geometry of the TFTs (notice that the semiconductor island is wider than the channel width, and that the overlaps are different for the conventional long channel, the conventional short channel, and the self-aligned TFTs).

C. AC performance

First the AC performance of the TFTs can be estimated by calculating the transit frequency f_T according equation 1 [30]:

$$f_t = \frac{g_m}{2\pi C_G} \tag{1}$$

here g_m is the transconductance and C_G is the gate capacitance. Both values are known from the DC characterization. Utilizing Eq 1, f_T is calculated to be $1.1\,MHz$ (conventional), and $3.7\,MHz$ (self-aligned) for long channel transistors, and $6.2\,MHz$ (conventional), and $56.9\,MHz$ (self-aligned) for short channel transistors. Here, it is worth mentioning that conventional as well as self-aligned flexible IGZO TFTs can reach higher f_T if the bias voltages and dimensions are individually optimized [24]. However, this would limit the comparability of the devices and is not pursued here.

The direct measurement of the AC performance (Fig. 4) was performed by acquiring the scattering parameters of the

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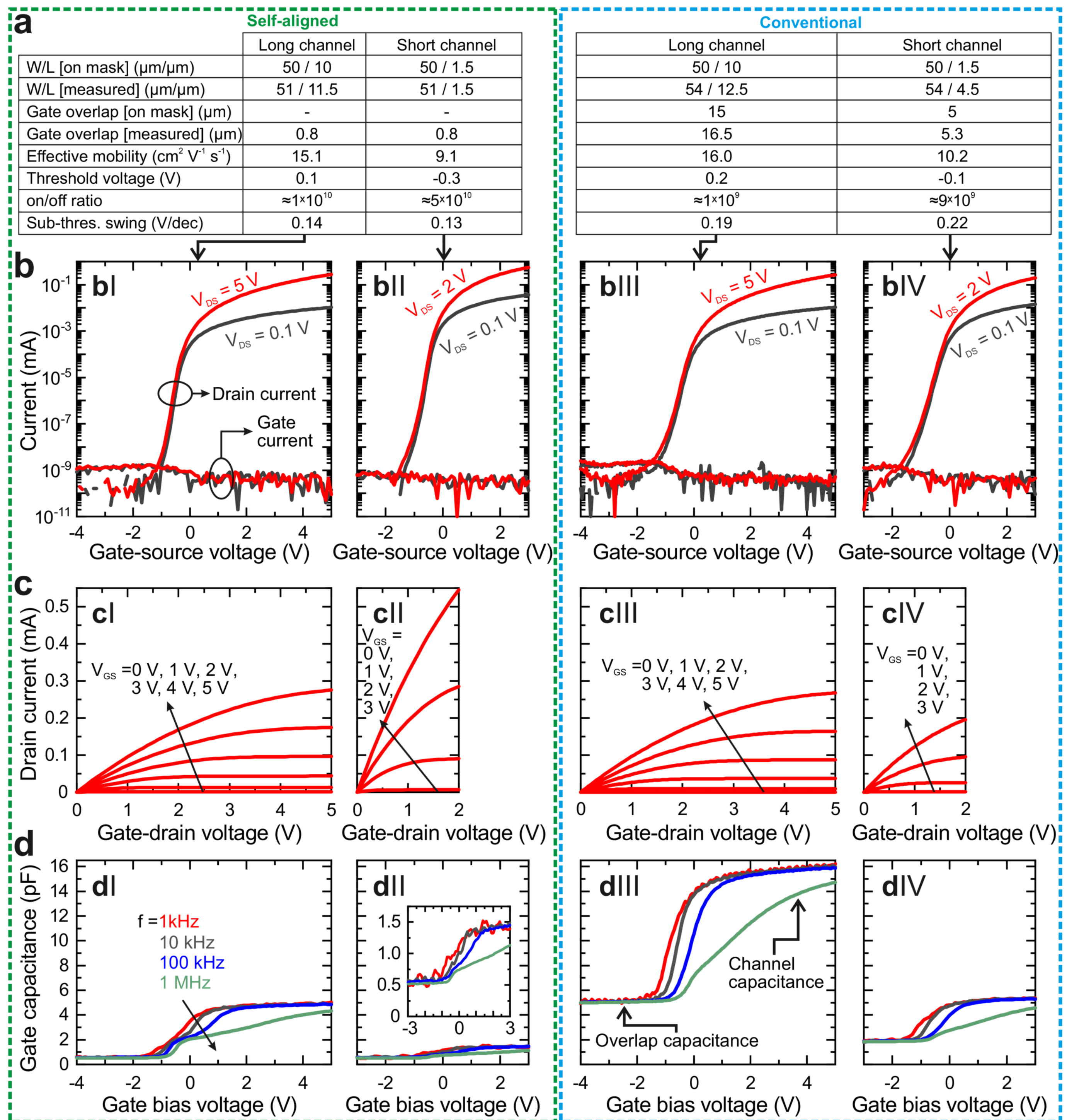

	Self-aligned Long channel	Self-aligned Short channel	Conventional Long channel	Conventional Short channel
W/L [on mask] (µm/µm)	50 / 10	50 / 1.5	50 / 10	50 / 1.5
W/L [measured] (µm/µm)	51 / 11.5	51 / 1.5	54 / 12.5	54 / 4.5
Gate overlap [on mask] (µm)	-	-	15	5
Gate overlap [measured] (µm)	0.8	0.8	16.5	5.3
Effective mobility ($cm^2 V^{-1} s^{-1}$)	15.1	9.1	16.0	10.2
Threshold voltage (V)	0.1	-0.3	0.2	-0.1
on/off ratio	$\approx 1 \times 10^{10}$	$\approx 5 \times 10^{10}$	$\approx 1 \times 10^{9}$	$\approx 9 \times 10^{9}$
Sub-thres. swing (V/dec)	0.14	0.13	0.19	0.22

Fig. 3. DC performance of flexible self aligned and conventional short and long channel TFTs. a) Summary of the geometrical parameters and the DC performance of various TFTs. b) Transfer characteristics (incl. gate leakage current) measured in the linear and the saturation regime. c) Measured output characteristics. d) Measured gate capacitance (extracted for different measurement frequencies while the source and drain contacts were connected).

TFTs using a Keysight E5061B ENA vector network analyzer and GSG probe tips. Here, DC bias voltages to one channel were applied by the network analyzer (port 1), while a DC bias to port 2 was applied utilizing an external bias-T and a Keysight SMU. Prior to any measurement, the system was calibrated using an open, short and 50 Ω load. During the measurements, the source was grounded, while port 1 and port 2 were connected to the gate and the drain of the TFTs. All measurements were performed at frequencies between 100 kHz and 500 MHz. Examples of the resulting scattering parameters for a self-aligned and a conventional TFT (measured at the same bias voltages of V_{GS}=V_{DS}=2 V) are shown in Figs. 4c and 4f. The S-parameters were then used to calculate the current gain h_{21} (Figs. 4a and 4d) [31]. Next, f_T

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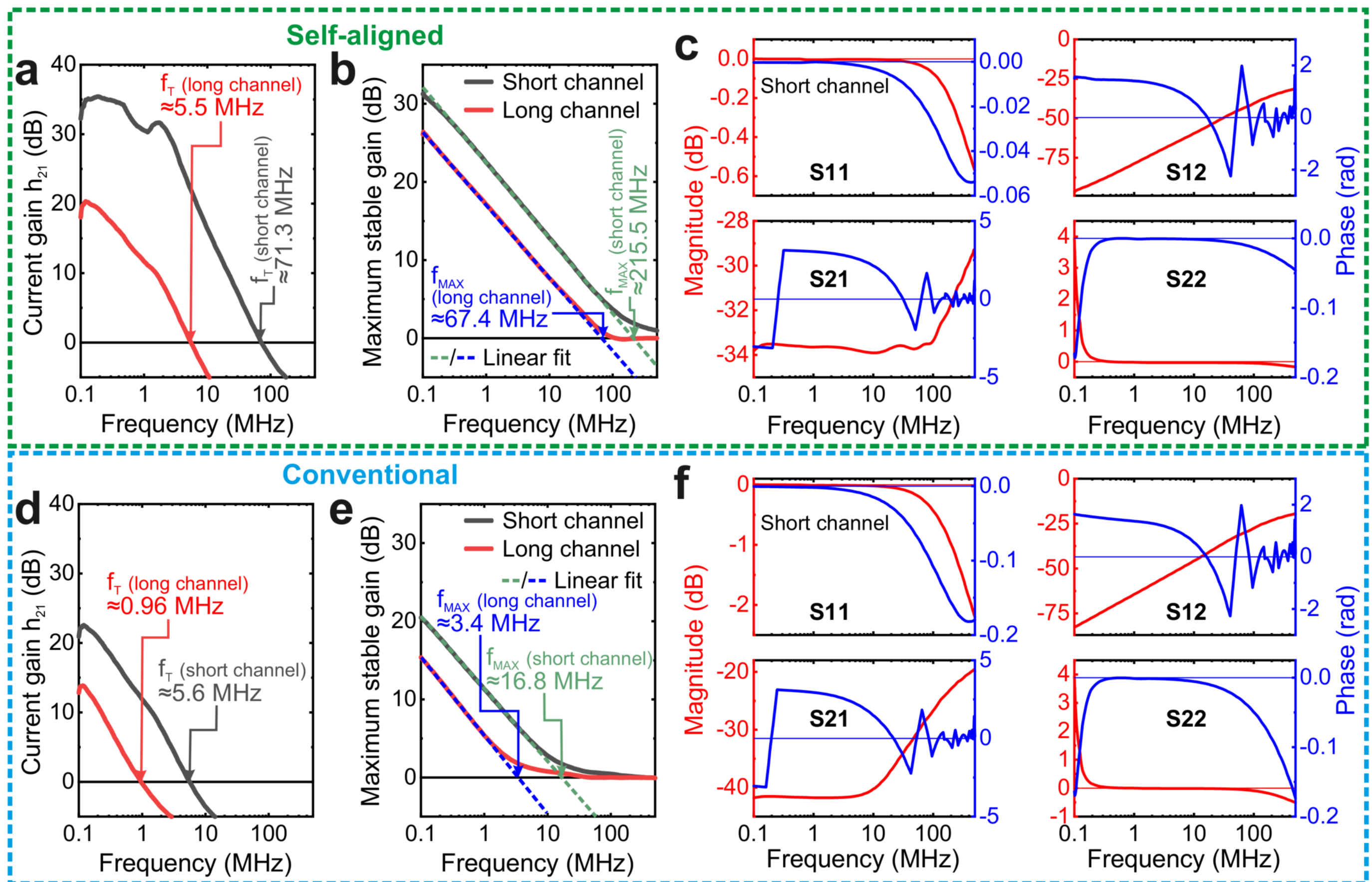

Fig. 4. TFT AC performance: a) Measured current gain, and resulting transit frequency of a long and a short channel self-aligned TFT. b) Measured maximum stable gain, and resulting maximum oscillation frequency of a long and a short channel self-aligned TFT. c) Representative s-parameters of a short channel self-aligned TFT used to determine the frequency performance. d) Measured current gain, and resulting transit frequency of a long and a short channel conventional TFT. e) Measured maximum stable gain, and resulting maximum oscillation frequency of a long and a short channel conventional TFT. f) Representative s-parameters of a short channel conventional TFT used to determine the frequency performance. The DC bias points were: V_{GS}=$3\,\mathrm{V}$, V_{DS}=$5\,\mathrm{V}$ (long channel TFTs), and V_{GS}=V_{DS}=$2\,\mathrm{V}$ (short channel TFTs).

was extracted as the unity gain frequency of the current gain. The experimental values for f_T are $0.96\,\mathrm{MHz}$ (conventional), and $5.5\,\mathrm{MHz}$ (self-aligned) for long channel transistors, and $5.6\,\mathrm{MHz}$ (conventional), and $71.3\,\mathrm{MHz}$ (self-aligned) for short channel transistors. These values are generally in very good agreement with the calculation. The only difference is observed for the short channel self-aligned TFT, this is due to an overestimation of the gate capacitance which could only be measured at frequencies $<1\,\mathrm{MHz}$. Finally, the S-parameters were also used to calculate the maximum stable gain (Figs. 4b and 4e) of the transistors [17]. It is used to determine the maximum oscillation frequency f_{MAX} of the TFTs. f_{MAX} is the frequency at which a power gain of unity can be reached, it is traditionally larger than f_T. The f_{MAX} extracted here are: $3.4\,\mathrm{MHz}$ (conventional), and $67.4\,\mathrm{MHz}$ (self-aligned) for long channel transistors, and $16.8\,\mathrm{MHz}$ (conventional), and $215.5\,\mathrm{MHz}$ (self-aligned) for short channel transistors, which are in line with the expectations.

IV. Conclusion

A new integrated fabrication process for the realization of conventional and self-aligned IGZO TFTs on a flexible polymer foil was investigated and demonstrated. The full process utilizes nine lithography masks plus self-aligned lithography based on backside illumination through the substrate. Long and short channel TFTs were fabricated to demonstrate the possibility of realizing TFTs with bespoke performance. The resulting substrate includes reliable conventional TFTs with effective mobilities up to $16\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, and self-aligned TFTs with a maximum oscillation frequency up to $216\,\mathrm{MHz}$, while the TFT gate capacitance can be tuned by more than one order of magnitude. Both types of TFTs were fabricated using the same metallic, insulating, and semiconducting thin-films deposited on a single flexible substrate. This integrated fabrication allows the direct comparison of the TFTs electrical DC and AC performance confirming the trends observed for similar TFTs fabricated on different substrates in the past. In the context of analog integrated circuits, which are particularly influenced by the performance of individual TFTs, it is suggested that self-aligned TFTs are used for high-speed circuits, while the higher reliability and effective mobility of conventional TFTs make them ideal building blocks for current mirrors or low-frequency, high-gain amplifiers. Finally, although designed with the nominally same channel dimensions on the lithography mask, the different source/drain manufacturing techniques of conventional and self-aligned TFTs result

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in significantly different final channel lengths on the substrate. This has to be considered when designing future integrated circuits based on conventional and self-aligned flexible TFTs.

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