3.93 MHz / 328 µW Dynamic Frequency Divider in Flexible a-IGZO TFT Technology

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***Abstract*—The implementation of a dynamic frequency divider in a fully-flexible amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) thin-film transistor (TFT) technology on a sub-15µm polyimide substrate is presented. This frequency divider is regenerative and is also known as a Miller divider. In this work, it is implemented using only a Gilbert cell with minimum-size LO transistors. Including the bias network, it has only 8 transistors. Using a 6 V supply voltage, it operates up to 3.93 MHz, consumes 328 µW, and has a speed over power figure-of-merit (FOM) of 12.0 MHz/mW. To the best knowledge of the authors, this FOM is the highest reported for circuits in this class of flexible TFT technologies.**

***Index Terms*—Dynamic frequency divider, flexible electronics, indium-gallium-zinc-oxide (IGZO), Miller frequency divider, thin-film transistors (TFT)**

I. Introduction

Flexible electronics has great potential to closely integrate into our daily lives. Wireless communication is essential for many of those applications. Amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) is one of the most promising semiconductors for fully flexible thin-film transistor (TFT) electronics, because it has a relatively high effective mobility and can be processed at low temperatures.

As a result, ISO-standard compliant, fully flexible RFID- and NFC-tags in a-IGZO TFT technologies have received great attention [1], [2]. Such tags need a frequency divider [1] to derive their clocks from the carrier signal of a wireless reader. A common division ratio is 128 for a carrier of 13.56 MHz. Realizing the frequency divider is very challenging because of at least two reasons. The speed of flexible thin-film transistors is limited in comparison to the carrier frequencies. Also, standard-compliant wireless tags are only allowed to consume a few tens of milliwatts. The required frequency divider alone can easily consume a large portion of that.

The presented Miller divider was implemented using minimum device dimensions for the LO transistors T_1 - T_4 in a 0.8 µm technology, with n-type metal oxide transistors based on a-IGZO. It was manufactured on a sub-15µm polyimide substrate on a commercial manufacturing line [3]. This work demonstrates that the presented circuit is more power efficient than previous works in similar technologies and that it can be used as the fourth and later stages of a frequency divider in a 13.56 MHz RFID- or NFC-tag.

This work was supported in part by the European Regional Development Fund (EFRE), in part by the Free State of Saxony, and in part by the DFG under projects WISDOM II and Coordination Funds 2 of SPP 1796 under grants 271795180 and 270774198. The presented circuits were fabricated by PragmatIC® in the FlexLogIC® *fab-in-a-box* manufacturing line.

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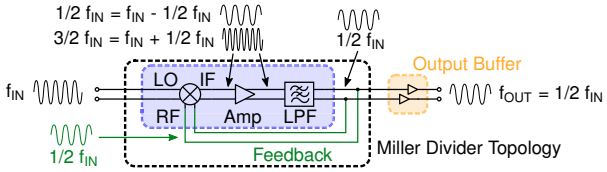

Fig. 1. Miller divider topology: mixer, amplifier, low pass filter, and feedback. The frequency components observed under proper operation are shown. [4]

II. Circuit Design

The Miller divider topology [4] divides the input frequency f_{IN} by 2. A system-level schematic is shown in Fig. 1. When the circuit divides correctly, mixer output IF has components $1/2\,f_{IN}$ and $3/2\,f_{IN}$. If the mixer does not introduce any phase shift, the low-pass filter (LPF) must attenuate $3/2\,f_{IN}$ by at least 9.54 dB. If phase shift is present, the minimum required attenuation for $3/2\,f_{IN}$ is in the range of 6.0 dB and 10.8 dB. The loop gain for $1/2\,f_{IN}$ has to be above unity. [5]

We implement the Miller divider topology as shown in Fig. 2, using only a Gilbert cell without a dedicated amplifier or LPF. The LO-port and the RF-port of the standalone Gilbert cell have a simulated voltage gain of 4 dB and 6 dB and a simulated bandwidth of 39 MHz and 26 MHz, respectively.

Let us consider a simplified case to illustrate the circuit operation. Assuming the LO transistors T_1–T_4 switch fully on and off without delay, the circuit alternates between two configurations, shown in Figs. 3(a) and 3(b), while cycling through four phases (i) – (iv):

Phase (i): The circuit is in configuration Fig. 3(a), while input $V_{\text{in n}}$ is low and $V_{\text{in p}}$ is high. IF_n and IF_p saturate towards high and low, respectively. The imbalance described below determines that node IF_n saturates towards high. *Phase (ii)*: Inputs $V_{\text{in n}}$ and $V_{\text{in p}}$ flip and the circuit switches to configuration Fig. 3(b). The divider circuit is now similar to two active inverting LPFs with an initial condition. It has a very small corner frequency of $f_{\text{LPF}} \approx 1/(2\pi \cdot R_{\text{G RF}} C_\text{n}) \approx 1.7\text{kHz}$. That means, amongst other things, the third harmonic $3/2\,f_{IN}$ is strongly attenuated and nodes IF_n and IF_p level out at their mean value $V_{\text{IF DC}}$. In practice, IF_n and IF_p initially overshoot $V_{\text{IF DC}}$, because the bias points of RF_n and RF_p slowly follow the swing of IF_n and IF_p. IF_n and IF_p do not quite settle

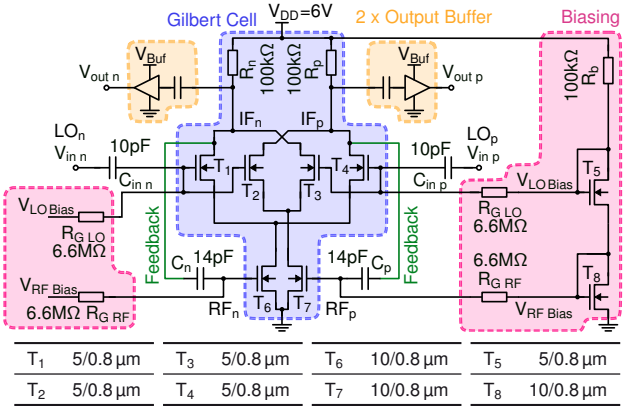

Fig. 2. Schematic of the implemented Miller divider. Transistor dimensions are given in channel width/length in µm. The output buffers are 4-stage ac-coupled common-source buffers.

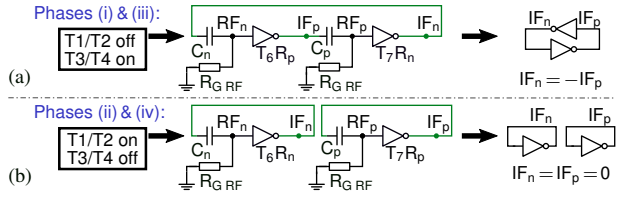

Fig. 3. Simplified circuit operation. (a) $V_{in\,n}$ = low and $V_{in\,p}$ = high. (b) $V_{in\,n}$ = high and $V_{in\,p}$ = low. The inverter symbol and T_xR_y stands for the common source stage formed by transistor T_x and load resistor R_y.

to $V_{IF\,DC}$ before the circuit transitions to the next phase. *Phase (iii)*: The circuit reverts to configuration Fig. 3(a) when inputs $V_{in\,n}$ and $V_{in\,p}$ flip back to low and high, respectively. IF_n and IF_p saturate again. This time the circuit is still unbalanced from the overshoot of the previous phase (ii). Therefore, IF_n and IF_p saturate to values inverted with respect to phase (i). *Phase (iv)*: Finally, inputs $V_{in\,n}$ and $V_{in\,p}$ flip again. Nodes IF_n and IF_p return to zero with an overshoot opposite to phase (ii), and the circuit cycles back to phase (i). As shown, the circuit amplifies signals only during phases (i) and (iii). Therefore, gain and bandwith requirements on the mixer are higher than compared to those on the mixer of a Miller divider that has a dedicated amplifer and low-pass filter.

Fig. 4 shows simplified qualitative waveforms for Fig. 3 and the simulated waveforms for the left circuit half of Fig. 2. The overshoot at the beginning of phases (ii) and (iv) is too small to be visible to scale. The divider fails at frequencies $f_{IN} < 150\,\text{kHz}$, because phases (ii) and (iv) are long enough for nodes IF_n and IF_p to settle so close to the mean $V_{IF\,DC}$ that IF_n and IF_p randomly saturate towards high and low during phases (i) and (iii). Any noise introduced into the feedback loop raises the minimum input frequency and has to be included during simulation. The impact of noise can be decreased by decreasing $R_{G\,RF}$. At higher frequencies the circuit fails to divide, because IF_n is increasingly delayed with respect to $V_{in\,n}$ and the loop gain falls below unity. The simulated upper limit for the input frequency versus V_{DD} is shown in Fig. 5(a) as a dashed red line. All simulations were done using a fitted BSIM4 transistor model.

The Gilbert cell and bias network use the same device

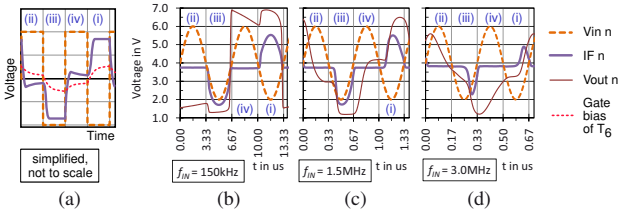

Fig. 4. (a) Simplified and (b) – (d) simulated waveforms $V_{in\,n}$, IF_n, $V_{out\,n}$ for the left half-circuit for input frequencies $f_{IN} = 150\,\text{kHz}$, 1.5 MHz, and 3 MHz. The phases (i) – (iv) of the simplified circuit opration are labeled in blue. RF_n (not shown) is virtually identical to IF_n plus a DC-offset.

dimensions. This configuration reduces the circuit's sensitivity to process variation. A bias network with a larger resistance and smaller power consumption could also be used.

The two output buffers are 4-stage ac-coupled common-source (CS) buffers [6], which have been integrated with the divider to ease its characterization. They have a gain, lower corner frequency, and upper corner frequency of 24 dB, 20 kHz, and 5.3 MHz, respectively. Their input impedance is 4 MΩ in parallel with the gate of a minimum-dimension transistor (channel width/length of 5/0.8 µm). In a practical application, the output buffers will be replaced appropriately, while maintaining the load imposed on nodes IF_n and IF_p. The current output buffers cause distortions (see Fig. 4). Therefore, internal signals IF_n, IF_p, RF_n, and RF_p cannot be observed directly. To mitigate these distortions, the gain of the buffers could be reduced by lowering the buffer supply voltage V_{Buf} or by adding source degeneration.

To design the circuit we start from $T_1 - T_4$ with minimum dimensions, because we target low power consumption. We assume $V_{GD} = 0\,\text{V}$ for all transistors and choose R_n and R_p such that the voltage accross them and $V_{DS\,1-4}$ of $T_1 - T_4$ equal $V_{DD}/3$. Minimum channel length is selected for T_6 and T_7. Their width is adjusted to satisfy $V_{DS\,6,7} = V_{DD}/3$. The resulting Gilbert mixer has an RF gain of around 3 dB more than its LO gain. At this point we verify that the RF voltage gain meets our target of at least 6 dB, which ensures with margin that the divider loop gain is above unity. If the gain requirement had not been met, we would first have increased the bias voltages and then R_n and R_p. $R_{G\,RF}$ and $C_n = C_p$ are chosen such that $f_{LPF} \approx 1/(2\pi \cdot R_{G\,RF}\,C_n)$ is smaller than the targeted minimum operating frequency.

The circuit speed can be increased by reducing R_n and R_p, and by increasing the gate bias voltages. This measure is limited by the linked reduction of gain and output dynamic range. The divider speed can also be increased by raising the supply voltage, if the application permits it.

III. Measurement

Circuit characterization is performed with differential sinusoidal and square wave input signals. The differential output signal is measured and analyzed with an oscilloscope. In the following we present all signal voltages as single-ended peak-to-peak values. If not otherwise specified, we use default operating conditions of supply voltage $V_{DD} = 6\,\text{V}$, buffer supply voltage $V_{Buf} = 7\,\text{V}$, and an input sine wave with $f_{IN} = 1\,\text{MHz}$, and $V_{IN\,PP} = 4\,\text{V}$.

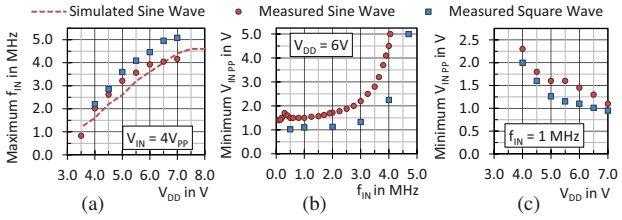

Fig. 5. (a) Measured and simulated maximum input frequency f_{IN} versus supply voltage $\mathrm{V_{DD}}$. (b) Measured minimum input voltage $\mathrm{V_{IN\,PP}}$ versus input frequency $\mathrm{f_{IN}}$ and (c) versus supply voltage $\mathrm{V_{DD}}$.

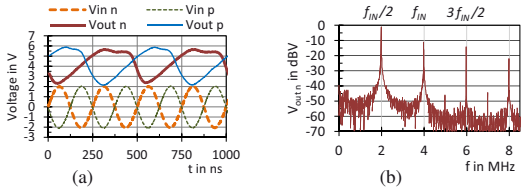

Fig. 6. (a) Measured waveforms for $f_{\mathrm{IN}} = 4\,\mathrm{MHz}$ and $f_{\mathrm{OUT}} = 1/2\,f_{\mathrm{IN}} = 2\,\mathrm{MHz}$ at $\mathrm{V_{DD}} = 7\,\mathrm{V}$ and (b) spectrum of waveform $\mathrm{V_{out\,n}}$.

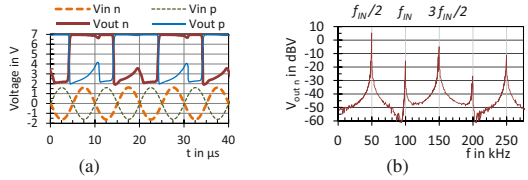

Fig. 7. (a) Measured waveforms for $f_{\mathrm{IN}} = 100\,\mathrm{kHz}$ and $f_{\mathrm{OUT}} = 1/2\,f_{\mathrm{IN}} = 50\,\mathrm{kHz}$ and (b) spectrum of waveform $\mathrm{V_{out\,n}}$.

Fig. 5(a) shows the measured and simulated maximum input frequency f_{IN} that is properly divided by 2 versus supply voltage V_{DD} at a constant input signal voltage $V_{\mathrm{IN\,PP}} = 4\,\mathrm{V}$. The divider operates properly down to around $f_{\mathrm{IN}} = 100\,\mathrm{kHz}$. A square wave input increases the maximum operation frequency compared to a sine wave, which is the expected behavior. From a supply voltage of $V_{\mathrm{DD}} = 7\,\mathrm{V}$, a square wave input up to $f_{\mathrm{IN}} = 5.1\,\mathrm{MHz}$ can be divided. The plot also shows that the simulation predicts the average maximum f_{IN} as a function of V_{DD} well, especially when considering that – as described below – we report the measurements for a circuit sample that performs 600 kHz above average.

Fig. 5(b) shows the minimum required input voltage $V_{\mathrm{IN\,PP}}$ for proper operation versus input frequency f_{IN} and Fig. 5(c) versus supply voltage V_{DD}. Measured waveforms and the respective spectra of output signal $V_{\mathrm{out\,n}}$ are shown in Fig. 6 for $f_{\mathrm{IN}} = 4\,\mathrm{MHz}$, $V_{\mathrm{DD}} = 7\,\mathrm{V}$ and in Fig. 7 for $f_{\mathrm{IN}} = 100\,\mathrm{kHz}$, $V_{\mathrm{DD}} = 6\,\mathrm{V}$. The spurs at 7 MHz and 9 MHz in Fig. 6(b) are an indication that the divider is operating close to its maximum frequency. The bumps in the output signals in Fig. 7(a) are caused by the capacitive coupling of the output buffers and can be observed in simulation in Fig. 4 for $f_{\mathrm{IN}} = 150\,\mathrm{kHz}$.

Fig. 8 shows the spread of maximum input frequency versus power consumption for 25 circuit samples and two supply voltages V_{DD}={6V,7V}. The large spread originates from process variation in combination with the high sensitivity of the mixer to transistor mismatch. The circuit sample that was used for the detailed characterization shown in Figs. 5 to 9

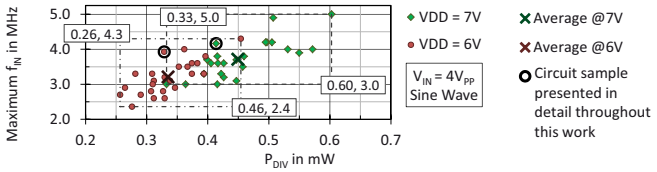

Fig. 8. Measured spread of maximum input frequency versus power consumption for 25 samples and two supply voltages $V_{\mathrm{DD}} = 6\,\mathrm{V}$ and $V_{\mathrm{DD}} = 7\,\mathrm{V}$. The bounds of the spread are marked by dashed lines and framed pairs of P_{DIV} in mW and f_{IN} in MHz for $V_{\mathrm{DD}} = 6\,\mathrm{V}$ and $_{\mathrm{DD}} = 7\,\mathrm{V}$.

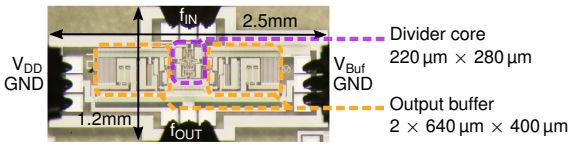

Fig. 9. Chip photo of Miller divider. The total chip area is 1.2 mm × 2.5 mm.

and Tables I and II is circled in black. In terms of speed it performs 600 kHz above average. It has a maximum input frequency of 3.93 MHz. The measured power consumption at $V_{\mathrm{DD}} = 6\,\mathrm{V}$ and $f_{\mathrm{IN}} = 3.93\,\mathrm{MHz}$, excluding the output buffers, is $P_{\mathrm{DIV}} = 328\,\mu\mathrm{W}$, of which 107 µW is consumed by the bias network. The output buffers consume 14.65 mW each. The single-ended input power is around 0.3 µW or −35 dBm.

The averages of power consumption and maximum frequency of all samples are 340 µW and 3.3 MHz for $V_{\mathrm{DD}} = 6\,\mathrm{V}$, and 450 µW and 3.70 MHz for $V_{\mathrm{DD}} = 7\,\mathrm{V}$. The simulated maximum frequencies (see Fig. 5(a)) are 3.6 MHz for $V_{\mathrm{DD}} = 6\,\mathrm{V}$ and 4.4 MHz for $V_{\mathrm{DD}} = 7\,\mathrm{V}$. This corresponds to a prediction accuracy of 8 % and 16 %, respectively.

Fig. 9 shows a chip photo of the Miller divider circuit.

IV. Comparison to the State of the Art

We use speed over power consumption as figure-of-merit (FOM), because the speed of a frequency divider f_{DIV} always has to be traded off with its power consumption P_{DIV}. A larger FOM indicates a more efficient frequency divider and is better.

$$\mathrm{FOM} = \frac{f_{\mathrm{DIV}}}{P_{\mathrm{DIV}}} = \frac{f_{\mathrm{D\text{-}FF}}}{P_{\mathrm{D\text{-}FF}}}. \tag{1}$$

Only very few frequency dividers in flexible a-IGZO thin-film technologies (TFT) have been reported. Therefore, in Table I, we also include two D-flip-flops (D-FF), which can be used to build a frequency divider that has a speed of $f_{\mathrm{D\text{-}FF}}$ and a power consumption of $P_{\mathrm{D\text{-}FF}}$. Some previous works focus on system-level aspects and do not report divider power consumption. We do not include them in the comparison, because the FOM cannot be calculated in these cases.

To broaden the data basis for the state-of-art comparison, we use the performances of flexible a-IGZO ring oscillators (RO). Reference [1] provides measurements that can be used to relate the speed $f_{\mathrm{D\text{-}FF}}$ of D-FF based frequency dividers to the stage delay τ_{INV} of a RO

$$f_{\mathrm{D\text{-}FF}} = \frac{1}{l \cdot \tau_{\mathrm{INV}}} \quad \text{with} \quad \tau_{\mathrm{INV}} = \frac{1}{2 \cdot f_{\mathrm{RO}} \cdot n}, \tag{2}$$

where data in [1] reveals that in practice l is in the range $l = [11,15]$. We use a small $l = 10$ for the comparison of the

TABLE I
COMPARISON TO FLEXIBLE D-FF BASED FREQUENCY DIVIDER [1] AND D-FFS [7], [8].
*THE POWER CONSUMPTION OF THE INDIVIDUAL D-FF DIVIDER IS NOT REPORTED, HOWEVER POWER CONSUMPTIONS OF RELATED RING OSCILLATORS AND A SYSTEM INCLUDING THE D-FF DIVIDER ARE. WE ESTIMATE $P_{\text{D-FF}}$ BASED ON THESE RELATED VALUES.

Semi.	Substrate	Ref.	Year	Circuit Topology	f_{DIV} or $f_{\text{D-FF}}$ in MHz	P_{DIV} or $P_{\text{D-FF}}$ in µW	**FOM = $\mathbf{f_{D\text{-}FF}}$ / $\mathbf{P_{D\text{-}FF}}$ in MHz / mW**	V_{DD} in V
a-IGZO	Polyimide	**This Work**	2020	Miller Divider	3.93	328	**12.0**	6
		[1]	2017	pCMOS Divider based on D-FF	13.56	2500*	5.4	3
IZO	Glass	[7]	2018	pCMOS D-FF w/ feedback	0.02	57.9	0.35	5
a-IGZO	Glass	[8]	2018	8-bit Shift Register based on D-FF	0.02	9.0	2.22	2

TABLE II
STATE-OF-ART AND FIGURE-OF-MERIT FOM OF THIS WORK AND OF FLEXIBLE RING OSCILLATORS.

Semi.	Substrate	Ref.	Year	n RO-Stages	P_{RO} in µW	f_0 in Hz	τ_{INV} in ns	Est. $f_{\text{D-FF}}$ in MHz	Est. $P_{\text{D-FF}}$ in µW	**FOM = $\mathbf{f_{D\text{-}FF}}$ / $\mathbf{P_{D\text{-}FF}}$ in MHz / mW**	V_{DD} in V
a-IGZO	Polyimide	**This Work**	2020	-	-	-	-	3.93	328	**12.0**	6
	PEN	[9]	2020	31	1500	1.0 k	16129	0.01	290	0.02	6
	Polyimide	[10]	2019	19	71	54.8 k	480	0.21	22	9.4	5
		[11]	2017	3	1700	3.04 M	55	1.82	3400	0.54	3
		[2]	2016	19	23820	910 k	29	3.46	7522	0.46	10
	Glass	[12]	2013	9	< 170	3.2 k	17361	0.01	< 113	> 5E-05	6
IZO	Glass	[13]	2017	11	201	132 k	344	0.29	110	2.65	5

presented divider to the state-of-art, because this overestimates $f_{\text{D-FF}}$. The RO stage delay τ_{INV} can be calculated from the reported oscillation frequency f_{RO} and the number n of stages [14]. We estimate the power $P_{\text{D-FF}}$ of a D-FF based divider from the reported total power P_{RO} of a RO

$$P_{\text{D-FF}} = m \cdot \frac{P_{\text{RO}}}{n}, \tag{3}$$

where $m = 6$ is an estimate based on the number of NAND- or NOR-gates that typically constitute a D-FF. Table II gives the estimated FOM for ROs. The presented Miller divider has the best figure-of-merit of FOM = 12.0 MHz/mW among all previous works considered in Tables I and II.

V. CONCLUSION

The presented implementation of a Miller divider with only a Gilbert cell has fewer degrees of freedom compared to other implementations that have a dedicated amplifier and LPF. The overall system considerations still hold, but details of the circuit operation differ. Most prominently, during 50 % of each cycle virtually all frequency components in the feedback loop are strongly attenuated. The presented circuit has only 8 transistors, including the bias network. It has the best speed over power figure-of-merit reported so far. Using a supply voltage of $V_{\text{DD}} = 6$ V, it consumes 328 µW and can divide 3.93 MHz, i.e. it has a figure-of-merit of 12.0 MHz/mW.

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