5 to 31 Hz 188 µW Light-Sensing Oscillator With Two Active Inductors Fully Integrated on Plastic

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Abstract-We present a low-power low-frequency oscillator that is fully integrated on a bendable plastic substrate using a-IGZO TFTs. Its purpose is the duty cycling of components of a wireless sensor tag to realize power savings. Additionally, the oscillator can directly be used as a light sensor. It oscillates between 5 Hz in the dark and 31 Hz under daylight, from a 5 V supply voltage. The measured light-sensitivity of the oscillation frequency is between 7.4 Hz/klx in the dark and around 1.7 Hz/klx in daylight. On average the frequency of oscillation changes by 58 %/klx. The required power is 188 µW. The presented design is a combination of the inductance-capacitance cross-coupled oscillator structure and two single-transistor active inductors, which enable high gain at low power levels in a small chip area. We analyze the circuit and derive design guidelines for minimizing the oscillation frequency, circuit area and power consumption. Finally, we report measurements including jitter and deduce implications for the accuracy of light measurements.

Index Terms—Active inductor (aL), amorphous indiumgallium-zinc oxide (a-IGZO), bendable, cross-coupled oscillator, flexible electronics, light sensor, plastics, thin-film transistor (TFT), wireless sensor

I. INTRODUCTION

Flexible electronics is currently undergoing significant development. They have a much lower carrier mobility than conventional silicon circuits, but they promise new properties. They can be fully bendable to the diameter of a hair [1], stretchable, foldable, transparent, ultra-lightweight, disposable, and bio-compatible, while being very affordable.

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Fig. 1. Simplified block diagram of targeted system structure for the bendable wireless sensor tag. [16]

Consequently, they potentially integrate with our surroundings and life much better than silicon electronics. Recent advances in the performance of bendable transistors now make their application in wireless communication systems possible. Examples for these advances are bendable amorphous indiumgallium-zinc oxide (a-IGZO) thin-film transistors (TFTs) with $f_{\text{max}} > 300 \text{ MHz}$ [2] and zinc oxide TFTs with $f_{\text{max}} = 2 \text{ GHz}$ fabricated on glass in a process compatible to flexible substrates [3]. Among bendable electronics, a-IGZO TFTs is one of the fastest technologies [4]. It provides carrier mobilities of around $15 \text{ cm}^2/\text{Vs}$, an f_t of 135 MHz [5], and an f_{max} of about 300 MHz [2]. Typically, a threshold voltage V_{TH} in the range from 0V to 2V is reported. The technology is compatible with a wide range of substrates. On a 50 µm polyimide substrate, circuits can be bent to a mechanical strain of 1.55 % [6]. Circuit reliability has been steadily improved [7] and fabrication costs are relatively low. They are already widely used in flat panel displays. Depending on the substrate, even higher mechanical strains are possible, e.g. 2.3 % on a 80 µm elastomeric substrate [8].

We are developing circuitry for a bendable active sensor tag, which can be attached to perishable goods for monitoring their environmental conditions. If for example the light exposure of a good surpassed the permissible limit, the tag sends an alert. The sensor element is of course not limited to light [9] and the possible scenarios are manifold. One very notable field of application is personal health care. Examples for other sensor elements are temperature [10], hall [11], [12], water and humidity [13], ionizing radiation, chemical [14], pressure [10], and strain [10], [15].

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The basic building blocks of the wireless sensor tag are shown in Fig. 1. Related to this goal, power supplies that could be integrated have been shown in [17], [18]. Analog-to-digital converters [19]–[21] as well as oscillators [22], [23] to read out sensor states have been demonstrated before. Also baseband signal synthesis for radio-frequency identification (RFID) tags has for example been published in [24].

The focus of this work is the low frequency oscillator. It is used to duty cycle the sensor and comparator sub-circuits to realize power savings. Additionally, it can directly be used as a light sensor. If the light sensitivity is however undesired, it can also be suppressed by means of transistor biasing conditions, the top metal layout, or packaging.

The targeted supply voltage for the wireless sensor tag is 5 V, because it is a good compromise of device endurance and the ability to deliver RF power from the circuitry. At this supply voltage, the estimated power consumption of the targeted sensor tag is 16 mW. The low frequency oscillator consumes 188 µW, the comparator 3 mW, the high frequency oscillator and mixer 6.8 mW [16], and the power amplifier 5 mW. The power consumption of sensors depends on their nature: as an example, a wet sensor requires 0.7 mW. Consequently, switching off the sensor and comparator saves 23 % power, which is also the upper limit of power savings by duty cycling these blocks. A more sophisticated system design could allow the high frequency oscillator and the mixer to be duty cycled as well, which would save even more power. Then however the receiver of the system would have to deal with the periodical abscence of the carrier.

A lower frequency of the oscillator and thus a lower duty cycling frequency results in a larger power saving, but reduces the update rate. Since power consumption is crucial for a wireless tag, we aim at a very low frequency of oscillation that is still acceptable for our application regarding update rate. At the same time we minimize circuit area as well as the number of transistors to improve matching, yield, cost and integratability. We also target a small power consumption and good jitter performance.

Typically such a low frequency oscillator requires one of or a combination of a large inductance, a large resistance, or a large capacitance. Any of which is at best challenging to integrate in a TFT technology in a small area and with a small tolerance. Particularly if large impedances are used to achieve long periods of oscillation, the jitter of the oscillator will be relatively high.

This difficulty can be avoided with a digital approach that combines a faster oscillator and a frequency divider. In contrast to conventional silicon circuits, the digital approach would however not be well suited for a-IGZO TFTs. For example the 3.4 MHz signal of the high frequency oscillator of the tag could be divided down to 13 Hz by a counter consisting of 18 D-flip-flops. The power and area requirements for this counter would however be in the order of 250 mW and 100 mm² respectively. These requirements are huge compared to the proposed low frequency oscillator, which needs only 188 μ W and 5.7 mm² respectively.

The remainder of this work is organized as follows. Section II presents the active-inductance capacitance (aL-C) crosscoupled oscillator circuit topology, analyzes its behavior and deduces design guidelines. Section III presents measurements and compares them to the predicted behavior. Section IV gives a comparison of state-of-art oscillators. Low frequency oscillators are rare among previous works. Therefore, fast oscillators are included in the survey. Section V concludes this work.

II. OSCILLATOR CIRCUIT

A. Application Requirements

The main application requirements and constraints for this work are 5 V supply voltage, targeted $f_0 = 15$ Hz, low jitter, low power consumption, fully integrated, and bendable. The oscillator has to serve two purposes:

- 1) It triggers switches S_1 and S_2 in Fig. 1, which switch the supply voltage to the sensor elements and the comparator at speed f_0 for a predefined, short time period t_{on} . Time t_{on} is determined by the characteristics of S_1 and S_2 . Consequently, they are only active at the low frequency f_0 and a small duty cycle $n_{S1} = t_{on} \cdot f_0$, where t_{on} is chosen as short as possible. This reduces the power consumption of the baseband part of the wireless sensor tag by up to 23 %.
- 2) The oscillator can itself be used as a light sensor, because its oscillation frequency is modulated by the incident light intensity. This is caused by varying drain currents of the TFTs when illumination changes [25]–[27]. In this application scenario the oscillator output is directly used as baseband signal. This leads to a simplified system structure compared to Fig. 1, without dedicated sensor elements and comparator. An additional benefit is that no technological steps for the manufacture of a photo-detector element are required. For this application of the oscillator, its jitter has to be low to achieve a small measurement error.

If this light sensitivity is however undesired it has to be suppressed.

The number of transistors and the required circuit area of the oscillator should be minimized to improve matching, yield, cost, and integratability.

B. Bendable a-IGZO TFT Technology

The oscillator is fabricated using n-type only, bottom-gate top-contact a-IGZO TFT technology without self-alignment on a bendable polyimide substrate as described in [28]. Fig. 2 shows the bent substrate containing, amongst other circuits, the oscillator. The technology offers a total of three metal layers [29]. The full potential of this technology regarding operation speeds is described in detail in [2], [5]. Implementation of metallic resistors is possible using the gate metallization; this however requires a large area of at least $30 \,\mu m^2/\Omega$. Consequently, active loads are relevant. Capacitors using the gate dielectric or a second dielectric layer as insulator. They require at least $230 \,\mu m^2/pF$. The implementation of integrated spiral inductors is not practical.



Fig. 2. Photo of bent polyimide film carrying a variety of a-IGZO TFT circuits. The inset magnifies the presented low frequency oscillator circuit.

C. Proposed Circuit Topology

To reach an oscillation frequency as low as 15 Hz while minimizing circuit area, power consumption and jitter, we propose an active-inductance (aL) capacitance (C) cross-coupled oscillator topology. It combines the inductance-capacitance (LC) cross-coupled oscillator topology with the single-transistor active-inductor sub-circuit, which has been presented and analyzed by us in [30] recently.

The behavior of the aL sub-circuits, as we will show, is defined by a capacitance and a large resistance that require respectively only 17% and 10% of the circuit area.

The aL circuit has been shown to enable a high gain at low power levels in a single amplifier stage. At the same time, the circuit conveniently allows defining bias currents. In this work we extend the work on the aL sub-circuit and demonstrate that the lower corner frequency of the active inductor can be designed to be as low as $f_1 = 5.4$ Hz while exhibiting an equivalent inductance L_p in the order of 4.8 kH, which allows exploiting its performance in a low frequency oscillator.

In the topology used in previous work [30] the frequency characteristics of the aL sub-circuit are partly defined by the drain-source leakage of two oppositely stacked MOS diodes M_8 and M_9 . Since the drain-source leakage cannot be controlled well, we modify the aL sub-circuit to instead rely on three series MOS diodes (T_{Ra1} , T_{Rb1} , and T_{Rc1} in Fig. 3a). Due to design rules, it is not possible to use a larger single diode instead.

The proposed structure also relies on drain-source leakage. Yet, it still provides an improvement regarding sensitivity to process variation and circuit area. In Sec. II-E we show that a low frequency of oscillation is achieved, if the resistance of $T_{Ra1} + T_{Rb1} + T_{Rc1}$ is large during the half-period in which the series of MOS diodes is biased reversely, i.e. $V_{DD} > W_1$. Their resistance during the other half-period, during which W_1 exceeds V_{DD} , is not relevant for the oscillation frequency. Consequently, an oppositely biased MOS diode is not needed. As a result, for the three series MOS diodes, the resistance per area is larger and the number of transistors that can be affected by process variation is half compared to the oppositely stacked MOS diodes used in [30].



Fig. 3. Low frequency oscillator schematics: (a) Transistor level schematic and (b) simplified schematic using the equivalent circuit from Fig. 4b for the analytic estimation of the oscillation frequency. Transistor dimensions are shown as channel width / length in μ m.

The full oscillator circuit including device dimensions is shown in Fig. 3a. To reduce jitter we implement two capacitances C₁ and C₂. Alternately, nodes V_1 and V_2 are high-ohmic (up to around 200 k Ω) and thus especially susceptible to noise. In particular during the high-ohmic half-periods C₁ or C₂ act as low pass filters to reduce noise. This noise would otherwise increase jitter by causing the cross couple to randomly trip late or early. The design also includes source follower output buffers T_{out1} and T_{out2}, which are needed during measurement to decouple the circuit characteristics from influences of the measurement setup.

In the following analyses and discussions, we assume low light condition (illuminance $E_V = 500 \text{ lx}$) and symmetry of the circuit, i.e. $T_1 = T_2$, $C_1 = C_2$, and so on. Consequently, we primarily discuss the behavior of the right half of the circuit, which applies equivalently to the left half. For circuit simulations we use the model described in [31], which has been fitted to low light condition ($E_V = 500 \text{ lx}$).

D. Active Inductor Sub-Circuit Analysis

It has been shown in [30] that sub-circuits aL1 and aL2 can each be modeled by the RLC-tank shown in Fig. 4a or by the equivalent RLC-tank shown in Fig. 4b. The characteristics of these RLC-tanks are shown in Figs. 4c and 5. For comparability to the previous work, the analyses are plotted for the same operating point. Since both RLC-tanks Fig. 4a and 4b are equivalent and model the active inductor sub-circuits, we use parameters of both RLC-tanks as well as parameters from the transistor level active inductor circuit in the following analysis. This enables more concise equations. The formula



Fig. 4. Active inductor equivalent circuits (a) + (b) and their characteristics (c) for the device dimension shown in Fig. 3a. Q_s is the Q-factor for series elements L_s and R_s . Q_p is the Q-factor of the parallel tank circuit shown in (b). $R_s = 28.7 \text{ k}\Omega$, $L_s = 4.8 \text{ kH}$, $C_p = 4 \text{ pF}$, and $R_b = 133.5 \text{ k}\Omega$. Equivalent circuit (a) has no frequency dependent parameters. Equivalent circuit (b) is frequency dependent.

for converting between parameter sets $(R_{1s}, L_{1s}, R_{1b}, C_{1p})$ and (L_{1p}, R_{1p}, C_{1p}) is given in [30].

The equivalent oscillator circuit schematic when using the aL model according to Fig. 4b is shown in Fig. 3b. This circuit topology resembles a cross-coupled LC oscillator and is known to oscillate if

$$(g_{mT1} \cdot R_{1p}) \cdot (g_{mT2} \cdot R_{2p}) > 1$$
 (1)

at a frequency of [32]

$$f_0 = \frac{1}{2\pi \cdot \sqrt{L_{1s} \cdot (C_{1p} + C_1)}} \cdot \sqrt{1 - \frac{R_{1s}^2 \cdot C_{1p}}{L_{1s}}},$$
 (2)

with the first term being the natural frequency of the LC oscillator and the second term describing the deviation from the natural frequency due to losses in R_{1s}. Inductance L_{1s} and resistance R_{1s} are elements of the equivalent model for subcircuit aL1 according to Fig. 4a. The transconductance of T₁ in the presented design (Fig. 3a) is $g_{mT1} \approx 0.1$ mS or higher. The resistance R_{1p}(f) of the aL1 sub-circuit is sufficiently large for all frequencies and V_{Load1} (see Figs. 4 and 5) for the CS stage to provide more than enough gain to satisfy (1). Our design goal was $(g_{mT1} \cdot R_{1p}) \cdot (g_{mT2} \cdot R_{2p}) > 2 \cdot 2$ down to 1 Hz, to have sufficient margin and to achieve low jitter. A higher gain is known to reduce the jitter of the oscillator.

The analysis according to [30] of the aL sub-circuits yields $L_{1s} = 4.8 \text{ kH}$ and $C_{1p} = 4.0 \text{ pF}$. Consequently, according to (2) the oscillation frequency of the circuit shown in Fig. 3b should be $f_0 = 130 \text{ Hz}$. This is however not in agreement with simulation and measurement by one order of magnitude. This error can be attributed to the strong dependency of the characteristics, in particular losses in R_{1s} , of the aL1 equivalent circuit on the voltage V_{Load1} . This V_{Load1} dependency is illustrated in Fig. 5c, which shows the resistance of the active inductor observed at dc and at the center frequency f_0 versus voltage V_{Load1} .





Fig. 5. (a) and (b) Simulated impedance of active inductor design, when looking from node V_1 or V_2 into active inductor aL1 or aL2 respectively. $f_{0 aL} = 1.1 \text{ kHz}$, $Z(f_{0 aL}) = 137.3 \text{ k}\Omega$. Lower corner frequency $f_1 = 5.4 \text{ Hz}$. Upper corner frequency $f_2 = 269 \text{ kHz}$. Data is shown for voltage $V_{load} = 1 \text{ V}$ and thus directly comparable to publication [30]. (c) Effect of V_{load} on the resistance of the active inductor.



Fig. 6. Extremely simplified schematic of the right half of the oscillator circuit.

E. Oscillation Frequency and Duty Cycle

Equation (2) does not predict the oscillation frequency well, because it is a small signal analysis. However instead, the circuit behavior and oscillation frequency f_0 can be estimated based on the transients of the charging process of C_{L1} more precisely. Fig. 6 shows an extremely simplified schematic of the right half of the oscillator circuit to illustrate the circuit operation and the following analysis. At some time capacitance C_{L1} has been discharged and voltage V_1 is low. C_{L1} is then charged via $T_{Ra1} + T_{Rb1} + T_{Rc1}$ for time t_{cha1} until voltage W_1 is high enough to switch on T_{L1} . This triggers the cross-couple (T_1, T_2) to trip. The same process then happens in the left branch and so on. Therefore we can calculate the frequency of oscillation f_0 by determining the charging time t_{cha1} . To do so, the start of charge voltage $V_{CL1,min}$ and the end of charge



Fig. 7. Simulated charging and discharging process of capacitor C_{L1} . The simulated frequency of oscillation is $f_0 = 13.5$ Hz. The bottom plot also shows the output voltage OutN if the circuit was connected to an oscilloscope $(1M\Omega||15pF)$.

voltage $V_{\text{CL1,max}}$ have to be determined first. The simulated waveforms for the charging and discharging process of the right half of the circuit are plotted in Fig. 7.

We assume that voltage $V_{CL1} = W_1 - V_1$ across C_{L1} is

$$V_{\rm CL1,min} = V_{\rm DD} - V_{\rm high1},\tag{3}$$

when charging C_{L1} starts, where V_{DD} is the supply voltage and V_{high1} is the output high level of common source stage T_1 .

The charging voltage (i.e. theoretical end-of-charge voltage after an infinite charging time) is

$$V_{\rm cha1,max} = V_{\rm DD} - V_{\rm low1},\tag{4}$$

where V_{low1} is the output low level of the common source stage T₁. The series resistance R_{cha1} for the charging process is the channel resistance of transistors $T_{\text{Ra1}} + T_{\text{Rb1}} + T_{\text{Rc1}} + (T_1 || T_{\text{L1}})$.

While the voltage across C_{L1} rises, the source voltage of T_{L1} follows the gate voltage. The gain of the common drain stage T_{L1} is given by

$$Gv_{\rm SF1} = \frac{g_{\rm m\,T1L} \cdot R_{\rm DS\,T1on}}{1 + g_{\rm m\,T1L} \cdot R_{\rm DS\,T1on}}.$$
(5)

Consequently, voltage V_1 rises for time t_{cha1} until it reaches $V_1 = V_{trip2}$ and the cross-couple trips. Where V_{trip2} is the gate voltage of T_2 required to cause T_2 to switch on and thus the cross-couple to trip. We estimate the voltage across C_{L1} at this point as

$$V_{\text{CL1,max}} = \frac{V_{\text{trip2}} - V_{\text{low1}}}{Gv_{\text{SF1}}} + V_{\text{CL1,min}}.$$
 (6)

If the common source stage T_2 is designed to have high gain and high driving capability V_{trip2} approaches the threshold voltage V_{TH} of T_2 , else it is higher. The charging time t_{cha1} can be modeled as

$$t_{\text{chal}} = -\tau_{\text{chal}} \cdot \ln\left(1 - \frac{V_{\text{CL1,max}} - V_{\text{CL1,min}}}{V_{\text{chal}} \max - V_{\text{CL1,min}}}\right), \text{ with } (7)$$

$$\tau_{\rm cha1} = R_{\rm cha1} \cdot C_{\rm L1}.$$
(8)

Equation (7) can be transformed to

$$t_{\text{chal}} = -\tau_{\text{chal}} \cdot \ln\left(1 - \frac{1}{Gv_{\text{SF1}}} \cdot \frac{V_{\text{trip2}} - V_{\text{low1}}}{V_{\text{high1}} - V_{\text{low1}}}\right), \qquad (9)$$

and further simplified using estimations $V_{\text{high1}} = V_{\text{DD}}$ and $V_{\text{low1}} = 0$ to

$$t_{\rm cha1} = -\tau_{\rm cha1} \cdot \ln\left(1 - \frac{1}{Gv_{\rm SF1}} \cdot \frac{V_{\rm trip2}}{V_{\rm DD}}\right). \tag{10}$$

 C_{L1} will then discharge across R_{dis1} , which is also the channel resistance of transistors $T_{Ra1} + T_{Rb1} + T_{Rc1} + (T_1 || T_{L1})$. Voltage $(V_{DD} - W_1)$ across MOS diodes $T_{Ra1} + T_{Rb1} + T_{Rc1}$ reverses on trip. Consequently, the discharging resistance R_{dis1} is smaller than the charging resistance R_{cha1} by a factor of around 10. Therefore, the frequency of oscillation f_0 is only defined by the durations t_{cha1} and symmetrically t_{cha2} of the charging processes of C_{L1} and C_{L2} as

$$f_0 = \frac{1}{t_{\text{cha1}}} + \frac{1}{t_{\text{cha2}}},\tag{11}$$

where the charging time t_{cha2} for the left branch can be determined equivalently to (7) and (8). The duty cycle *n* is given by the following equation and is obviously 50 % for all symmetric circuits.

$$n = \frac{t_{\rm cha1}}{t_{\rm cha1} + t_{\rm cha2}}.$$
 (12)

Consequently, the duty cycle n_{S1} of the supply voltage to the sensor elements and comparator via switches S_1 and S_2 could not be controlled by the presented oscillator directly. Hence, S_1 and S_2 are implemented edge-triggered and self-opening after the programmed time t_{on} . The effective duty cycling n_{S1} of the supply voltage by S_1 and S_2 is given by $n_{S1} = t_{on} \cdot f_0$.

 R_{cha1} , C_{L1} , Gv_{SF1} , V_{high1} , V_{low1} , and V_{trip2} can be deduced from the device dimensions given in Fig. 3a. R_{cha1} and C_{L1} are designed to be 150 MΩ and 1100 pF respectively. The gain of the common drain stage T_{L1} is $Gv_{SF1} \approx 0.34$, with $R_{DS T1on} \approx 3 k\Omega$ and $g_{m T1L} \approx 0.17$ mS. The tripping voltage is $V_{trip2} \approx 0.8$ V. We estimate $V_{high1} = V_{DD}$ and $V_{low1} = 0$. From (9) we can then calculate $f_0 = 2/t_{cha1} = 18.9$ Hz. Determining the high and low levels more precisely yields $V_{high1} \approx 4.6$ V and $V_{low1} \approx 0.1$ V and consequently $f_0 = 2/t_{cha1} = 19.6$ Hz. The simulated frequency of oscillation is $f_0 = 9.1$ Hz.

Simulations further confirm that the dimensions of T_1 and T_{L1} can be further optimized to yield an even slower oscillations at virtually the same power consumption and circuit area. These modifications do however reduce the gain of the CS stages and are therefore expected to affect jitter. Consequently, we have chosen the device dimensions shown in Fig. 3a.

F. Light Sensitivity and Power Consumption

The circuit's frequency of oscillation $f_0(E_V)$ is modulated by the illuminance E_V , mainly because the channel resistances of transistors $T_{Ral} + T_{Rb1} + T_{Rc1}$ change [33]. The change of resistance in turn affects the frequency of oscillation, which we have shown above in Sec. II-E.



Fig. 8. Measured drain current versus illuminance of four transistor dimensions. The bias condition was V_{GS} =1 V and V_{DS} =1 V.

The effect of illuminance on the drain current depends on the bias condition. Its light sensitivity is shown for one condition in Fig. 8. Please note that this particular measurement was done on transistors from a different, earlier fabrication than the presented oscillator circuits. The data therefore deviates from the transistor performance in the presented oscillator, yet clearly shows the impact of illuminance.

The total average power consumption P_{tot} of the circuit can be considered to have four components. The power P_{CL} to charge and discharge C_{L1} and C_{L2} , and the power P_C to charge and discharge C_1 and C_2 , which are both frequency dependent. Two frequency independent terms are the dc power P_{TL1} related to the dc drain current in T_{L1} , and the power consumption P_{buf} of the unloaded output buffers.

 P_{TL1} is around 200 µW at a supply voltage of $V_{DD} = 5 V$ and represents around 99 % of P_{tot} . Consequently, according to [33], P_{tot} should increase by about 10 % with an increase of illumination from dark to daylight due to an increase in the drain current of T_1 and T_{1L} . The faster cycle of charging and discharging C_{L1} , C_{L2} , C_1 , and C_2 will not effect P_{tot} notably, since the power consumption $P_{CL} + P_C$ for this process, as given by the following equations, is only in the order of 40 nW + 120 nW.

$$P_{\rm C} = P_{\rm C1} + P_{\rm C2} = 2 \cdot \frac{1}{2} \cdot f_0 \cdot \left(V_{\rm high1} - V_{\rm low1}\right)^2 \cdot C_1 \qquad (13)$$

$$P_{\rm CL} = P_{\rm CL1} + P_{\rm CL2} = 2 \cdot \frac{1}{2} \cdot f_0 \cdot V_{\rm CL1,max}^2 \cdot C_{\rm L1}$$
(14)

 P_{buf} is around 1.8 μ W. If both outputs of the circuit are loaded with an oscilloscope channel each, as shown below in Sec. III, additional 25 μ W are required. This power is delivered to the oscilloscope.

The presented circuit configuration has been optimized for a large light sensitivity. If however a stable and light independent oscillation frequency is desired, the light sensitivity can be suppressed in three ways. Obviously, packaging and housing of the oscillator can be made from an opaque material. Secondly, the top metal layer in the circuit can be used to cover the TFTs thus reducing the influence of the environmental light on the channel resistance. Lastly, the effect of light on the channel resistance depends considerably on the biasing condition of the transistor. Contrary to the presented configuration of the oscillator circuit, this can be used to reduce light sensitivity. The same effect is also the reason why the frequency of oscillation can be affected by light by around 600% while at the same time the power consumption is only affected by around 10%.

All three ways are selective and can suppress light sensitivity where needed. Covering circuits with top metal, as well as the transistor biasing conditions are obviously selective. Packaging can also be selective, for example when circuits are packaged by laminating them with barrier films. The used films can be opaque, transparent, and mixed. Also, they can have windows cut open. Therefore, the light sensing elements can be exposed while the remaining circuitry is shielded from light.

G. Frequency Reproducibility

The actual frequency of oscillation of fabricated circuits is affected by process variations. The major effect of process variations are global and local differences in threshold voltage V_{TH} . To quantify the influence of threshold voltage variation we use Monte Carlo simulation. We assume the threshold voltage to be normally distributed with a sigma of $\sigma_{Vth} = 50 \text{ mV}$, which is based on the measured threshold voltage distribution of 50 a-IGZO TFTs [34]. The variance is relatively large in our case, because shared equipment is used for the fabricated in an established stable process and it is very likely that various uncontrolled substances are introduced into the circuit layers during fabrication. Fig. 9 shows the results of the Monte Carlo simulations.

H. Design Guidelines

The values V_{trip2} , V_{high1} , V_{low1} , V_{DD} , and τ_{cha} are given directly by or can be deduced from the oscillator design and the chosen device dimensions in Fig. 3a. Therefore, we can use above equations and insight to formulate the following design guidelines, which aim to minimize frequency of oscillation f_0 , circuit area, power consumption, and jitter. The following still assumes circuit symmetry.

- The frequency of oscillation f_0 can be lowered with a larger C_{L1} : $f_0 \propto 1/C_{L1}$ [ref (7) and (8)]. This increases the circuit area by around 230 μ m²/pF.
- The frequency f_0 can be lowered by increasing the channel resistance of $T_{Ra1} + T_{Rb1} + T_{Rc1}$. Their aspect ratio W/L can be reduced and more transistors can be added in series. This increases the circuit area. This also effectively reduces the charging and discharging current through C_{L1} , which increases the negative effect of possible electromagnetic immissions on the noise and thus jitter of the oscillator.
- The frequency f_0 can be lowered slightly by increasing the channel resistances of $(T_1 || T_{L1})$. The effect on f_0 is however small, because R_{cha1} is dominated by $T_{Ra1} + T_{Rb1} + T_{Rc1}$. These changes can reduce the output swing.
- Mainly the dimensions of transistors T_{L1} and T_1 determine the power consumption of the circuit. The drain current of T_{Ra1} is negligible. Therefore, to minimize power consumption the drain current of T_1 has to be



Fig. 9. Reproducibility of the frequency of oscillation and the duty cycle determined by Monte Carlo simulation for low light condition ($E_V = 500 \text{ lx}$) with a sample size of 2140. We assumed the threshold voltage to be normally distributed with a sigma of $\sigma_{Vth} = 50 \text{ mV}$. Subfigure (a) shows the distribution of the frequency of oscillation, (b) shows the distribution of the duty cycle, and (c) shows the correlation of frequency and duty cycle.

minimized. The limit for this optimization is the condition given in (1). This also implies a reduction of the gain of the CS stage, which will affect jitter and reduce the output swing.

- The frequency f_0 can be lowered by increasing V_{trip2} [ref (7)], which implies reducing the gain of the CS stages, which is limited by the condition given in (1), will affect jitter, and reduce the output swing.
- A superficial interpretation of (10) might indicate that the frequency of oscillation increases with V_{DD} . However the relationship between f_0 and V_{DD} is complex, because V_{trip2} depends on V_{DD} . Instead an increase in V_{DD} affects V_{trip2} such that the frequency of oscillation decreases. Also the normalized output voltage will deacrease with a decreasing V_{DD} (ref. Fig 13b).
- The average power consumption P_{tot} can be reduced by reducing the aspect ratios W/L of transistors T_1 and T_{L1} simultaneously. However, this modification reduces the gain of the CS stage, which consequently affects jitter.
- The transistors are the main source for low frequency noise in the proposed circuit. Reducing their aspect ratios W/L reduces their 1/f noise [35], which benefits jitter. At the same time this will reduce f_0 and power consumption in most cases. This however also implies a reduction of the gain of the CS stage, which will in turn affect jitter. Consequently, no general design guideline regarding 1/f noise and jitter can be given.

III. MEASUREMENT

The fabricated oscillator circuit is shown in Fig. 10. The measurement setup is shown in Fig. 11. We conduct all measurements on a wafer prober that is equipped with a controllable light source and a lux meter. The whole circuit and all its transistors are illuminated uniformly. No transistor is cover by a metalization layer and the circuit is measured uncovered. Output signals OutN and OutP are recorded by an oscilloscope. The waveform is recorded for intervals of 30 s, and subsequently concatenated and analyzed on a PC to extract the frequency of oscillation f_0 and the cycle-to-cycle (C2C) jitter ΔT_{C2C} .



Fig. 10. Micrograph of low frequency oscillator circuit.



Fig. 11. Measurement setup for low frequency oscillator.

A. Waveform and Frequency of Oscillation

Fig. 12 shows the measured output signals OutN and OutP in comparison to the simulated OutN for a supply voltage of $V_{\text{DD}} = 5 \text{ V}$. The measured frequency of oscillation at low light condition ($E_{\text{V}} = 500 \text{ lx}$) is $f_0 = 9.1 \text{ Hz}$, while the simulation predicted an oscillation frequency of $f_0 = 13.5 \text{ Hz}$. The measured duty cycle is 48 %. It deviates from the predicted 50 % due to mismatch of the left and right branch.

The fall and rise times of each output signal differ by a factor of around 10. This is due to the design of the commondrain output buffer, which we primarily designed for low power consumption. Output OutN is driven up by transistor



Fig. 12. Measured and simulated waveform (a) of low frequency oscillator circuit at a supply voltage of $V_{\text{DD}} = 5.0 \text{ V}$ and an illuminance of $E_{\text{V}} = 500 \text{ lx}$. The measured frequency of oscillation is $f_0 = 9.1 \text{ Hz}$. The extracted duty cycle is 48 %. The simulated frequency of oscillation is $f_0 = 13.5 \text{ Hz}$. Magnifications (b) and (c) illustrate the measured rise and fall times, which are around 50 µs and 500 µs respectively.

 T_{out1} , which has a width to length ratio of $W_{Tout1}/L_{Tout1} = 10$. The output is pulled down by the oscilloscope and transistor T_{B1} . The width to length ratio of T_{B1} is $W_{TB1}/L_{TB1} = 2.5$, also its gate source voltage is tied to zero. Consequently, the pull-down capability of T_{B1} and the oscilloscope together is significantly smaller compared to the driving capability of T_{out1} . This imbalance has no effect on the internal nodes and the behaviour of the oscillator. Balancing rise and fall times is possible, but would result in a larger dc power consumption, slower rise and fall times, or a more sophisticated output buffer. For our target system symetry is not required and the measured fall and rise times are sufficiently steep.

Fig. 13a shows the measured frequency of oscillation vs. supply voltage $V_{\rm DD}$ in the dark. The circuit can oscillate from a supply voltage of $V_{\rm DD} \ge 0.47$ V. As expected f_0 decreases with an increase of the supply voltage. Consequently, the supply voltage can be changed to control the frequency of oscillation from 4 Hz to 110 Hz. At the nominal supply voltage of $V_{\rm DD}$ the frequency of oscillation f_0 changes with a change in supply voltage by $k \approx -2$ Hz/V. Obviously, $V_{\rm DD}$ changes also effect the output voltage levels and the power consumption at the same time. Fig. 13b shows these two characteristics under no light. The dc power ranges from 2 μ W for V_{DD} = 0.5 V and $f_0 = 109$ Hz, to 188 μ W for the nominal supply voltage V_{DD} = 5.0 V and $f_0 = 5.3$ Hz, and up to 332 μ W for V_{DD} = 6.0 V and $f_0 = 4.0$ Hz.

B. Light Sensitivity and Power Consumption

Fig. 13c shows the measured frequency of oscillation f_0 and the extracted light sensitivity vs. the illuminance E_V of the circuit. We determine the light sensitivity from the slope of the f_0 measurement. Consequently, light sensitivity is plotted for the intermediate E_V values of the f_0 measurement. On average the frequency of oscillation changes by 58 %/klx. The relative change in frequency of oscillation from no light to $E_V = 500 \, \text{lx}$ is as much as 91 %. The light sensitivity is largest for the dark condition and reduces towards brighter lighting conditions. This is a desired behavior, as this allows its usage as a light sensor across a broad range of lighting conditions and also because the human eye behaves similarly. The measurements show a slight but reproducible increase in light sensitivity around $E_V = 9 \, \text{klx}$. However, according to our predictions the light sensitivity should decrease monotonically.

The power consumption is dominated by the drain current of T_{L1} and behaves fairly like the data presented in [33]. When changing the illumination from dark to daylight the power consumption rises by only 10 μ W from 188 μ W to 198 μ W.

C. Jitter and Measurement Error of Illuminance

The histogram of the measured cycle-to-cycle jitter ΔT_{C2C} is shown in Fig. 14 for a total measurement time of about 2 min. Assuming the jitter is normally distributed, it's standard deviation can be estimated from Fig. 14 to be $\sigma_{C2C} = 150 \,\mu\text{s}$. When the oscillator is used as light sensor, this directly translates into the standard deviation of the random measurement error of the illuminance E_V . With the characteristics shown in Fig. 13c, $\sigma_{C2C} = 150 \,\mu\text{s}$ is equivalent to $\sigma_{EV} = 0.2 \,\text{klx}$ for darkness and to $\sigma_{EV} = 0.6 \,\text{klx}$ under daylight.

IV. COMPARISON TO THE STATE-OF-ART

Oscillators are basic building blocks for realizing a wealth of functionalities. Still, only very few low frequency oscillators operating below 1 kHz have been reported. The majority of oscillator circuits published over time in flexible electronics have been ring oscillators. In contrast to this work, their predominant purpose is demonstration of the performance of a flexible technology. In these cases the objective usually is minimum delay per stage. Unfortunately, in this context many times the power consumption has not been reported. Despite the importance of oscillators as a basic block only very few oscillators of other topologies have been demonstrated, and even less with the goal to achieve a particularly low f_0 . Among the compared oscillators only [22], [36] target slow operation.

Regarding jitter performance no data from previous works using a-IGZO technologies was available to us. However, a state-of-art 1 Hz ultra-low-power silicon oscillator [47] is commercially available. It is designed for mobile devices and wearables. The device is a sophisticated solution that integrates a high-quality micro-electro-mechanical system (MEMS) resonator as frequency reference. A configurable divider is driven by a phase-locked loop (PLL) based on this reference. Finally, the output of this divider is deliverd as clock output by an ultra-low power driver. Factory trimming is used to guarantee a frequency stability of 100 ppm within a temperature range



Fig. 13. Measured characteristics of oscillator circuit: (a) Oscillation frequency f_0 under no light, (b) normalized output voltage, and power consumption versus supply voltage V_{DD} under no light. (c) Oscillation frequency f_0 and light sensitivity versus illuminance E_V at a supply voltage of $V_{DD}=5 V$.

 TABLE I

 Comparison of state-of-art oscillator circuits in a-IGZO TFT technology and selected oscillators in other technologies.

Semiconductor	Substrate	Reference	Year	Circuit Topology, Notes	$V_{\rm DD}$ in V	f_0 in Hz	P in µW
a-IGZO	Polyimide	This work	2018	aL-C Cross-Couple	0.5	109	2
	2			-	5	5	188
		[36]	2018	Relaxation	+/-5	500	700
		[16]	2017	3-Stage Ring	3	3.04 M	1700
					4	3.44 M	3200
		[17]	2015	3-Stage pCMOS Ring	6	52.1 k	-
					2	7 k	-
		[37]	2011	11-Stage Ring	20	94.8 k	-
		[38]	2016	13-Stage bootsrapped pCMOS Ring	2	152	-
					20	364 k	-
		[24]	2016	19-Stage pCMOS Ring	0.5	28 k	2.03
					10	910 k	238200
	Glass	[39]	2010	5-Stage Ring	25	640 k	-
						2.1 M	-
		[40]	2013	9-Stage Ring	6	3.2 k	< 170
		[41]	2015	7-Stage pCMOS Ring, BCE BA a-IGZO	20	6.51 M	-
		[42]	2014	11-Stage Ring, dual gate a-IGZO	20	780.6 k	-
				11-Stage Ring, single gate a-IGZO		334.1 k	-
IZO	Glass	[43]	2017	PUC pCMOS 11-Stage Ring	5	132 k	201
ZnO	Glass	[44]	2016	LC Oscillator	7	35.3 M	56000
a-Si:H	-	[45]	2009	5-Stage Ring	6	30 k	2
Organic	Polyimide	[22]	2014	RC Oscillator, $C = 7 nF$	2	5	-
		[18]	2015	5-Stage Ring	12	1.5 k	< 2200
	PET	[46]	2015	5-Stage Ring	20	1.4 k	-

of -40°C to 85°C and a supply voltage range of 1.5 V to 3.63 V. This oscillator has a jitter of 35 ns and a core power consumption in the order of $3 \mu W$ compared to 150 μ s and 188 μ W respectively in this work.

In Table I we give an ample comparison of oscillator circuits in a-IGZO technology. The comparison is grouped by substrate, because fabrication processes on glass can potentially employ higher temperatures, which will improve a-IGZO performance dramatically. We also include two selected works using other metal-oxide technologies, one amorphous silicon technology, as well as three organic technologies for comparison. The circuit we present in this work has the lowest frequency and is among the circuits that consume the least power.

In Fig. 15 we arrange the data from Table I to show frequency of oscillation over supply voltage and power consumption. These plots illustrate that among the oscillators in metal oxide technology, the presented oscillator has the lowest oscillation frequency from the smallest supply voltage and the lowest power consumption at the same time.



Fig. 14. Histogram of measured cycle-to-cycle jitter ΔT_{C2C} . Applied supply voltage is V_{DD} = 5 V. The frequency of oscillation is $f_0 = 9.1 Hz$.



Fig. 15. State-of-art comparison of the frequency of oscillation f_0 of the oscillator circuits listed in Table I versus supply voltage and power consumption. Other MO refers to the IZO and ZnO based metal oxide (MO) technologies.

V. CONCLUSION

In this work, we have presented and analyzed an activeinductance (aL) capacitance cross-coupled oscillator. Its oscillation frequency can be modulated by illumination in the range from 5 Hz to 31 Hz for darkness to daylight from a 5 V power supply, while it consumes between 188 μ W and 198 μ W. The oscillation frequency also depends on the supply voltage. The minimum supply voltage to start oscillation is 0.47 V. The frequency of oscillation as well as the normalized output voltage scales well for supply voltages above 2 V. The circuit can sustain a supply voltage of up to 6 V. For this voltage range and in the dark, the frequency of oscillation ranges from 109 Hz down to 4 Hz, while it consumes between 2 μ W and 332 μ W respectively.

The active inductor (aL) sub-circuit has been instrumental to achieve this performance. Previous works mostly target fast oscillation speeds. In contrast to that, we have targeted a slow and stable oscillation at low power consumption in a small circuit area. The purpose of the presented oscillator is to dutycycle components of a wireless sensor tag to achieve power savings. We have simulated as well as analyzed the circuit behavior and deduced design guidelines to minimize oscillation frequency, power consumption, and jitter, which is directly related to the random error for illuminance measurements. The presented results have been confirmed by measurements. Additionally, the oscillator can directly be used as a light sensor without additional read-out circuitry. If this light sensitivity is undesired, it can be suppressed by means of transistor biasing conditions, the top metal layout, or packaging.

The demonstrated oscillator circuit is not the slowest possible configuration of the presented aL-C cross-coupled topology, but was specifically designed to achieve application requirements of $f_0 = 15$ Hz from $V_{DD} = 5$ V, low power consumption, and low jitter. By following the design guidelines we have presented, the power consumption and f_0 could be even further reduced by sacrificing jitter or increasing the circuit area or both.

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