Flexible In-Ga-Zn-O based circuits with two and three metal layers: Simulation and Fabrication study

G. Cantarella, K. Ishida, *Member, IEEE,* L. Petti, *Student Member, IEEE,* N. Münzenrieder, *Member, IEEE,* T. Meister, *Member, IEEE,* R. Shabanpour, C. Carta, *Member, IEEE,* F. Ellinger, *Senior Member, IEEE* G. Tröster, *Senior Member, IEEE* and G.A. Salvatore

***Abstract*—The quest for high-performance flexible circuits call for scaling of the minimum feature size in Thin-Film Transistors (TFTs). Although reduced channel lengths can guarantee an improvement in the electrical properties of the devices, proper design rules also play a crucial role to minimize parasitics when designing fast circuits. In this letter, systematic Computer-Aided Design (CAD) simulations have guided the fabrication of high-performance flexible operational amplifiers (opamps) and logic circuits based on Indium-Gallium-Zinc-Oxide (IGZO) TFTs. In particular, the performance improvements due to the use of an additional third metal layer for the interconnections has been estimated for the first time. Encouraged by the simulated enhancements resulting by the decreased parasitic resistances and capacitances, both TFTs and circuits have been realized on a free-standing 50 µm thick polymide foil using three metal layers. Despite the thicker layer stack, the TFTs have shown mechanical stability down to 5 mm bending radii. Moreover, the opamps and the logic circuits have yielded improved electrical performance with respect to the architecture with two metal layers: gain-bandwidth-product (GBWP) increased by 16.9 %, for the first one, and propagation delay (t_{pd}) decreased by 43 %, for the latter one.**

***Index Terms*—Indium-Gallium-Zinc-Oxide, flexible electronics, flexible circuits, Thin-Film Transistors (TFTs), metallization.**

I. Introduction

SINCE several decades, the progress of modern electronics has been linked to the scaling of the minimum feature size. This results in higher integration density, improved performance, and also in reduction of cost and dissipated power. This trend does not only concern silicon technology, but it also embraces flexible electronics. Here, the device scaling is strongly limited by process constraints: low temperature fabrication ($T_{max} < 200$ °C), limited photolithography resolution and substrate stability. Furthermore, to realize complex flexible circuits, many other parameters should be taken into account. From a design prospective, optimized layout (such as short interconnection lines or multiple metal layers) are required to reduce the parasitics (inductances, capacitances and resistances) and thereby increase the circuit speed [1], [2]. From a technological point of view, digital logic requires low threshold voltages V_{TH} and subthreshold swing SS, which determine the minimum gate-source voltage at which the transistor is in the on-state and the switching behavior of the circuit, respectively. On the other hand, for radiofrequency applications, a high cut-off frequency F_C and subsequently a large transconductance g_m, are needed for high performances [3], [4], [5], [6].

In this paper, we present the performance of two flexible circuits, an opamp and a digital circuit for mechanical switch control, based on amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) TFTs. Oxide semiconductors, and in particular amorphous a-IGZO, provide electron mobility $\mu_{eff} > 10\,\mathrm{cm}^2/\mathrm{Vs}$ [7], well above the standard values obtained for organic materials and amorphous-Si [8], [9]. After modeling all the transistor parameters for DC and AC characteristics [10], we studied the implementation of the two circuits using two metals layers (1^{st} metal: gate layer, 2^{nd} metal: source, drain and interconnections) and three metals (1^{st} metal: gate layer, 2^{nd} metal: source and drain, 3^{rd} metal: interconnections) for the first time (see Fig. 1a). Considering the decrease of the parasitics (capacitance and resistance) and the consequent improvement in the device performance in the latter case, we fabricated these devices on a free-standing 50 µm thick polymide foil. Despite the thicker layer stack, TFTs with three metal layers show high mechanical stability down to radii of 5 mm. Moreover, as a proof of the more suitable design using three metal layers, the opamp shows improvement of the gain-bandwidth-product (GBWP) up to 16.9 %, whereas the logic circuit exhibits an improvement of the propagation delay (t_{pd}) up to 43 %, with respect to a layout with only two metal layers.

II. Design and Fabrication

The modeling of a-IGZO TFTs for circuit design is based on our previous work [10]. As a first step, the device performance was simulated using two and three metals layers (and same layout) by Keysight ADS software and the parasitic capacitances C_p and resistances R_p were extracted. Considering the effective resistance of each metal layer (M1, Chromium as gate metal: 1.08 x $10^{-6}\,\Omega$ m; M2, Chromium/Gold/Chromium as source and drain metal: 8.6 x $10^{-8}\,\Omega$ m; M3, Titanium/Gold as interconnection metal: 7.2 x $10^{-8}\,\Omega$ m), their thicknesses (see Fig. 1a), the relative permittivity and thickness of the Al_2O_3 dielectric layers ($\epsilon_r \approx 9.51$, $\mathrm{thickness}_{2Metals-layout} = 25$ nm, $\mathrm{thickness}_{3Metals-layout} = 25$ nm + 80 nm = 105 nm) and a metal crossing of 40 µm x 40 µm, which is used for every wire intersection, we extracted a parasitic capacitance $C_{p-2Metals}$

Manuscript received .... G.Cantarella, L. Petti, G.A. Salvatore and G. Tröster are with the Institute for Electronics at the Swiss Federal Institute of Technology Zürich, Zürich, 8092, Switzerland. N. Münzenrieder is with Sensor Technology Research Center School of Engineering and Informatics at the University of Sussex, Richmond 3A7, Falmer, Brighton, BN1 9QT, United Kingdom. K. Ishida, T. Meister, C. Carta and F. Ellinger are with the Circuit Design and Network Theory, Technische Universität Dresden, Dresden 01069, Germany (corresponding email:giuseppe.cantarella@ife.ee.ethz.ch).

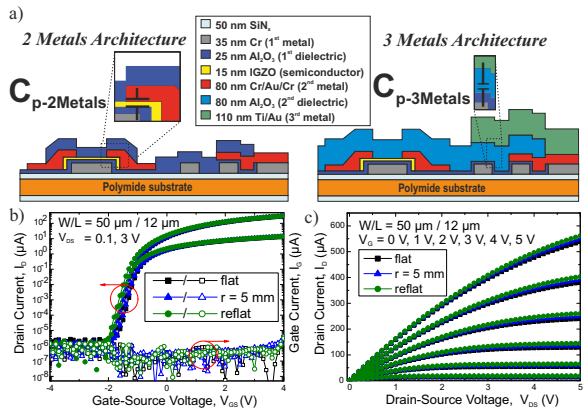
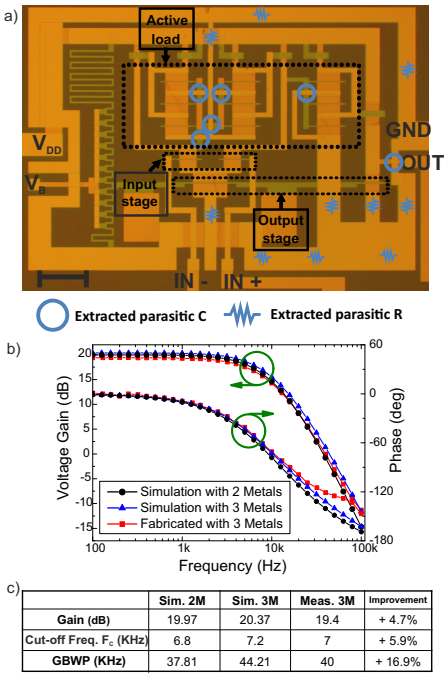


Fig. 1. (a) Cross section of flexible circuits based on a-IGZO TFTs fabricated with two metal layers and three metal layers on a free-standing 50 µm thick polymide foil; the parasitic capacitances C_p (in the insets) are calculated for both architectures; (b) transfer and (c) output characteristics of a three metals architecture a-IGZO TFT while flat, bent to r = 5 mm and reflattened.



	Sim. 2M	Sim. 3M	Meas. 3M	Improvement
Gain (dB)	19.97	20.37	19.4	+ 4.7%
Cut-off Freq. F_c (KHz)	6.8	7.2	7	+ 5.9%
GBWP (KHz)	37.81	44.21	40	+ 16.9%

Fig. 2. Operational amplifier fabricated with 13 a-IGZO TFTs. (a) Optical micrograph with three metal layers (scale bar 400 µm) with the physical position of the extracted parasitic resistive and capacitive components; (b) frequency response of the opamp in three different cases: simulated with two metals, simulated with three metals and fabricated with three metals; (c) summary of the amplifier performances for the three different cases. The "Improvement" column refers to the parameter variation from two metals simulated architecture to a three metals simulated one.

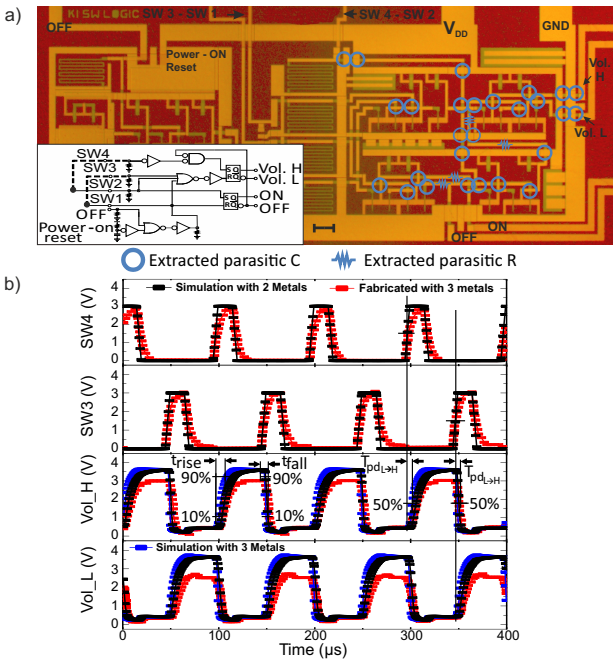
of 6.7 pF in the two metals structure and $C_{p-3Metals}$ of 1.6 pF for the three metal one (see Fig. 1a). As a consequence, the use of an additional 80 nm thick Al_2O_3 passivation layer combined with a third metal layer and considering same layouts in the CAD simulations reduces the parasitic capacitance of each wire crossing by 76 % and thereby the time constant RC, which limits the circuit speed. To verify the results of the above simulations, we fabricated TFTs and two circuits, an opamp and a digital circuit, implementing the three metals structure. The two layer process [11] is modified by depositing the additional 80 nm thick Al_2O_3 layer (by a Picosun Sunale R-150B Atomic Layer Deposition ALD), structuring the vias by wet etching and depositing a third metallization layer of Ti/Au (10/100 nm). The maximum process temperature is 150 °C and the total device thickness is 345 nm. Although other materials, such as SiN_x or SiO_x, could guarantee lower dielectric constants for the interconnections, we chose Al_2O_3 to guarantee a good interfacial quality between the semiconductor and the second dielectric, as well as an high fabrication compatibility with the layers underneath.

The IGZO TFTs were electrically characterized on free standing polymide foil, showing a saturation mobility of $17.38\,cm^2/Vs$, a V_{TH} of −1.04 V and SS equal to 0.137 V/dec. As proof of the unchanged electrical performances of the IGZO TFTs, the extracted parameters are in line with previous works where only two metal layers were employed [11], [12]. Afterwards, the TFTs were mechanically characterized at different bending radii. To investigate the bendability of the TFTs with a three metal architecture, the free standing polyimide foil tape was attached to a rod using a double side tape (thickness t_{tape} = 120 µm and Young's modulus E_{tape} = 10 MPa). Transfer and output characteristics of a TFT while flat, bent to a radius of 5 mm and then reflattened are shown in Fig.1b and 1c. Using the model developed in [13], the bending radius of 5 mm corresponds to a tensile strain of 0.55 %. In this case, the minimum bending radius depends rather on the substrate thickness (50 µm) than on the device one (345 nm). As a result, the TFT stays functional while bending parallel to the gate channel is applied, with parameters variation similar to the two metals device structure [11]. Furthermore, dynamic bending experiments were performed to evaluate the TFT parameters variations. Transfer and output characteristics have been measured at 0, 100, 250, 500 and 1000 cycles (not reported here) showing no significant degradation and, consequently, high mechanical stability, even in the case of a thicker device stack.

III. Circuits

Fig. 2a shows the micrograph of the opamp. It consists of 13 a-IGZO based TFTs grouped in a differential pair at the input, active loads in a pseudo-CMOS configuration and an output stage. The parasitic capacitances C_p and resistances R_p were extracted by the layouts and their values calculated by Keysight ADS software. Moreover, their physical position is shown in Fig. 2a. By choosing a layout with 40 µm wide metal lines, the extracted parasitic capacitances and resistances range from 1.6 pF (calculated for a minimum metal crossing) to 28.1 pF and from 3.7 Ω to 194 Ω, respectively. In this circuit, the origin of parasitic capacitances has to be referred to interconnection lines and wire crossing, while the parasitic resistances are due to internal metal paths in the layout. The opamp fabricated with 3 metal layers is characterized and its frequency response is shown in Fig. 2b. As summarized in Fig. 2c, the extracted parameters are usefully exploiting the benefits of a third metallization layer in combination with the thick passivation layer. In particular,

the comparison of the simulations with two and three metals (Fig. 2c, column "Improvement") highlights an increase of the gain (+4.7 %), resulting by the decrease of the parasitic resistance R_p, an enhancement of the bandwidth (+5.9 %), due to the reduction of the dominant pole of the parasitic C_p, and an improvement of GBWP (+16.9 %), affected by both parasitic components. Moreover, the parameter extraction for the experimental opamp shows results coherent with the simulation. Apart for the gain (equal to 19.4 dB), cut-off frequency F_c of 7 kHz and GBWP of 40 kHz show good agreement with the simulated parameters. The effect of the three metals architecture is further proved by the realization of a digital circuit for mechanical switch control. It consists of 32 TFTs forming 9 logic gates (4 inverters, 1 AND gate, 2 NOR gates and 2 S-R latches) (see Fig. 3a). The circuit detects the state of each inputor (SW1, SW2, SW3 and SW4) and holds the state at the output (Vol_L and Vol_H). Since each interconnection line and wire crossing corresponds to a parasitic capacitance, and also due to an higher device complexity, the difference between two and three metal layers is more evident. Indeed, improving the device architecture, and consequently decreasing the parasitic capacitance C_p and resistance R_p, has a strong impact on parameters, such as rise time t_{rise}, fall time t_{fall} and propagation delay t_{pd}. The output signals for the simulated device with two and three metals and for the one realized with three metals, are shown in Fig. 3b. The extrapolated values for the three metal layers architecture are $C_{p-3Metals}$, ranging from 1.6 pF to 52.3 pF, and $R_{p-3Metals}$, from 1 Ω to 11.8 Ω. As summarized in Fig. 3c, going from a two metal layer architecture to a three metal layer one, the rising and falling times of the input signals decrease by 36 % and 31 %, respectively. Similarly, the propagation delays t_{pd} (from high H to low L and from low L to high H) exhibit a sensible decrease of 40 % and 43 %. Apart for the t_{fall} where the experimental value is affected by process variations, the parameters extracted for the circuit fabricated with three metal layers (t_{rise} and t_{pd} from L to H and from H to L, equal to 12 ns, 7.5 ns and 3 ns, respectively) show good agreement with the simulated ones. The accuracy of the model (namely the variance between the parameters extracted by the simulated three metals architecture and the experimental ones) is mainly due to the device complexity. Passing from the operational amplifier (13 TFTs for a total circuit area of 7.8 mm^2) to the digital circuit (32 TFTs for a total circuit area of 23.7 mm^2), possible issues during the fabrication can occur and increase the difference between the simulated results and the experimental ones.



c)

	Sim. 2M	Sim. 3M	Meas. 3M	Improvement
t_{rise} (10%→90%) (µs)	15.5	9.9	12	- 36%
t_{fall} (90%→10%) (µs)	3.5	2.4	5.3	- 31%
t_{pd} (L→H, 50%→50%) (µs)	10.1	6.1	7.5	- 40%
t_{pd} (H→L, 50%→50%) (µs)	3.7	2.1	3	- 43%

Fig. 3. Logic circuit for mechanical switch control: (a) optical picture and schematic (in the inset) of the device with three metal layers (scale bar 300 µm) with the position of the extracted parasitic resistive and capacitive components; (b) time response of the circuit and (c) summary of the performances in three different cases: simulated with two metals, simulated with three metals and fabricated with three metals. The "Improvement" column refers to the parameter variation going from two metals simulated to a three metals simulated architecture.

IV. Conclusion

To our best knowledge, we have shown the first study on how proper circuit design rules combined with multiple metallization can have a key role in the realization of fast flexible thin-film circuits with high mechanical stability. After simulating and estimating the parasitic components using two metals or three metals structures, we have fabricated TFTs and circuits with a thick passivation layer (Al_2O_3, 80 nm) and a third metal layer (Ti/Au, 10/100 nm). Despite the thicker layer stack, the TFTs have shown unchanged mechanical stability and capability to be electrically characterized down to 5 mm bending radii (in static condition) and up to 1000 cycles (in dynamic condition). Moreover, the novelty of the fabrication and characterization of an opamp and a logic circuit (implemented with 13 and 32 a-IGZO TFTs, respectively) using three metal layers have highlighted notable performance improvements. In particular, by reducing the parasitics C_p and R_p, the opamp shows an increase of the gain (+4.7 %), of the bandwidth (+5.9 %), and of GBWP (+16.9 %), together with one of the highest complexity ever achieved within similar circuits based on metal oxide semiconductors [7]. Furthermore, the logic circuit for mechanical switch control has been fabricated for the first time on a flexible substrate and yields a reduction in all the delays (average decrease in the order of 38 %). Taking advantage of the high circuit complexity that can be reached, these results pave the way to further boost the circuit performance in the field of flexible electronics.

Acknowledgment

This study was supported by the SNF/DFG DACH FFlexCom project: Wireless Indium-Gallium-Zinc-Oxide Transmitters and Devices on Mechanically Flexible Thin-Film Substrates (WISDOM), SNF grant number 160347.

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