A Transistor Model for a-IGZO TFT Circuit Design Built upon the RPI-aTFT Model

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***Abstract*— This paper presents a compact transistor model for circuit design in a flexible amorphous indium gallium zinc oxide (a-IGZO) thin-film transistor (TFT) technology. The presented model is technology specific and builds upon the Verilog-A Rensselaer Polytechnic Institute amorphous silicon TFT (RPI-aTFT) model. On the basis of extensive device characterization, we introduce appropriate new equations and parameters that enable an accurate and efficient behavioral representation of a-IGZO TFTs. In this work, we address the modelling of short channel effects, the scalability for channel lengths from 5 µm to 50 µm, as well as the presence of process variation. Using this model, a Cherry-Hooper amplifier is designed, analyzed, implemented in a flexible a-IGZO TFT technology, and characterized. Finally, to validate the presented transistor model, we compare circuit simulations and measurements of the Cherry-Hooper amplifier circuit. The amplifier provides a voltage gain of 9.5 dB and has a GBW of 7.2 MHz from a supply voltage of 6 V. The simulation using our new compact transistor model resembles the measured characteristics very well. It predicts a voltage gain of 10.4 dB and a GBW of 7.0 MHz.**

Keywords*— *Integrated flexible amplifiers; modeling; thin-film transistors; TFT; a-IGZO; InGaZnO; flexible electronics; wearable electronics; analog circuits; amplifiers

I. Introduction

Flexible thin-film transistors (TFTs) are increasingly interesting for various applications such as bendable RFID tags, solar energy harvesting, and biomedical sensors [1-4]. Among the known semiconducting materials suited for flexible TFT technologies, amorphous indium gallium zinc oxide (a-IGZO) is one of the best candidates [5], because of its high field-effect mobility > 10 cm^2/Vs [6], the low-temperature fabrication (below 150°C) [7] and its bendability down to a diameter of 50 µm [8]. These characteristics make a-IGZO one of the most promising candidates for the realization of large-area flexible electronic systems [5]. In this work we focus specifically on the a-IGZO TFT devices presented in [2], which are fabricated using well-known photo lithography. Fig. 1 shows the cross-section of these transistors.

A compact TFT model is essential to design circuits efficiently. Previously, we have proposed the use of the SPICE Level 3 MOSFET model [9], because it is unlicensed and easily available in many circuit simulators. However, when employed for a-IGZO TFT circuit simulation the achievable accuracy and convergence speed are limited.

More accurate and faster compact models tailored to the simulation of TFT devices of various semiconducting materials are available. Works [10, 11] present such models, which are mainly physics based. One of them is the Rensselaer Polytechnic Institute amorphous silicon TFT (RPI-aTFT) model [11], which is available in a number of circuit simulators. This model is based on a unified and continuous description of the charge sheet density, which allows developing continuous expressions of the currents, and the small- and large-signal parameters. It uses physics-based parameters as well as empirical parameters suitable to model effects observed in amorphous silicon TFTs. Consequently, it can be fitted to a-IGZO TFT devices more accurately than other TFT models and than the previously proposed SPICE Level 3 MOSFET model. However, it still has shortcomings with respect to device dimension scalability.

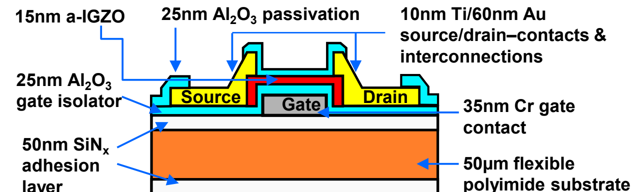

Fig. 1. Cross-section of flexible bottom-gate a-IGZO TFT [2].

In this work, to develop a behavioral a-IGZO TFT model, we extend the RPI-aTFT model by new parameters and equations. We also validate our a-IGZO TFT model by the comparison of measurements and simulations results of a fully flexible Cherry-Hooper amplifier in a-IGZO TFT technology.

II. Device Modelling

The a-IGZO TFT model proposed in this section overcomes limitations of the previously published model [9] with respect to device dimension scalability, convergence speed in the transient simulation, short-channel effect prediction, as well as scalability of I_D.

A. Underlying standard RPI-aTFT Model

The universal compact model developed at the Rensselaer Polytechnic Institute (RPI) for amorphous silicon TFTs [11], has been implemented in Verilog-A for computer aided design (CAD) tools. As for other TFT models, the field effect mobility in the RPI-aTFT model is a power function of the gate voltage overdrive [10-12]. It is however superior to earlier models especially for down-scaled TFT devices, because it takes into account effects caused by localized energy states in the bandgap of the thin-film. As a result, threshold voltage, field-effect mobility, leakage currents, the kink effect, and drain current above threshold are predicted more accurately. The implementation of the RPI-aTFT model in the Tiburon Design Automation [13] design kit, has eight geometrical and technological parameters (C_{gdo}, C_{gso}, T_{ox}, ε, $ε_I$, I_{ol}, R_d, R_s), seven trap distri-

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TABLE I. KEY MODEL PARAMETERS OF STANDARD RPI-aTFT MODEL, ADDITIONAL PARAMETERS OF PROPOSED MODEL, AND FITTING RESULTS.

Parameter	Description	Short model	Long model	Remarks	Unit
L	Length	≤12	≥12	Device dimension	μm
W	Width	50	50	Device dimension	μm
α_{Sat}	VDS, sat parameter	0.75	0.75	Fitted	--
δ	Transition parameter	8.5	8.5	Fitted	--
γ	Power law mobility	0.07	0.07	Fitted	--
G_{Min}	Minimum density of deep states	1.0E23	1.0E23	Fitted	--
M	Knee shape parameter	1.828	2.592	Fitted	--
μ_{Band}	Conduction band mobility	0.0019	0.0019	Fitted	m^2/Vs
I_{ol}	Zero bias leakage	1.0E-10	1.0E-10	Fitted	A
σ	Minimum leakage current	2E-9	2E-9	Fitted	A
V_0	Characteristic voltage for deep states	0.12	0.12	Fitted	V
V_{fb}	Flat band voltage	0.01	0.01	Fitted	V
E_l	Act energy of hole leakage	0.35	0.35	Process given	--
E_μ	Field effect mobility act energy	0.1	0.1	Process given	--
ε	Rel. dielectric const. of substrate	3.4	3.4	Process given	--
ε_I	Rel. dielectric const. gate insulator	9.5	9.5	Process given	--
T_{ox}	Thin-oxide thickness	25E-9	25E-9	Process given	m
R_d & R_s	Drain/Source contact resistance	By (4)	By (4)	Extended/Parameterized	Ω
C_{gdo} & C_{gso}	G-D/G-S capacitance	By (5) and (6), L_{ov}=5|μm	By (5) and (6), L_{ov}=5|μm	Extended/Parameterized	F
Def_0	Dark Fermi level	By (3): a = -11857, b = 0.76, L_{min}=5μm	By (3): a = 2950, b = 0.65, L_{min}=12μm	Extended/Parameterized	--
V_{to}	Zero-bias threshold voltage	By (1): P_{Vr}=1	By (2): P_{Vr}=1	Extended/Parameterized	V

bution and intrinsic layer quality related parameters (Def_0, G_{Min}, V_0, E_l, E_μ, μ_{Band}, V_{fb}), and more fitting parameters. Table I lists the key parameters of the standard RPI-aTFT model as well as the new additional parameters and fitted values of the a-IGZO TFT model proposed in this work.

B. Proposed a-IGZO TFT Model

Fig. 2 shows measured threshold voltage V_{th} of the a-IGZO TFT devices with channel lengths from 5 μm to 50 μm for a gate-source voltage V_{GS} of 5 V, respectively. The extracted threshold voltage depends on the channel length. It has a minimum at a channel length L of 12 μm and is significantly larger towards shorter and longer channels. However, the standard RPI-aTFT model cannot represent any channel-length dependency of the threshold voltage. In this paper, we tackle the modelling of this characteristic by binning in combination with adding equations to the standard RPI-aTFT model.

To realize binning, we determine one set of model parameters for short-channel devices (L ≤ 12 μm) and a second set of model parameters for long-channel devices (L ≥ 12 μm), while we guarantee continuity at L = 12 μm. Consequently, in the following we use channel length L_{REF} = 12 μm and channel width W_{REF} = 50 μm as reference dimension. The two sets of model parameters will be referred to as *short model* and *long model*. Additionally, we amend the zero-bias threshold voltage V_{to} of the standard RPI-aTFT model by equations (1) or (2) for the short and the long model respectively.

$$V_{to} = P_{Vr} \times \left\{ 0.35\,V \times \left(1 + \frac{L_{REF}}{L}\right)^{\left(\frac{L}{L_{REF}}\right)} - 0.15\,V \right\} \quad (1)$$

$$V_{to} = P_{Vr} \times 0.55\,V\,, \quad (2)$$

where L and $P_{Vr} > 0$ are the channel-length and the process variation factor, respectively. Unfortunately threshold voltage V_{th} variations occur very frequently in prototype processes and are difficult to address in a purely physical model [14, 15].

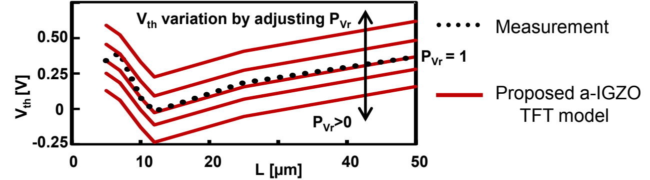


Fig. 2. Measured and simulated threshold voltage V_{th} versus channel length L. Also the influence of the process variations parameter P_{Vr} is shown.

Consequently, we introduce parameter P_{Vr} for use in statistical simulations of threshold voltage variations due to process variations. Throughout this work we will use P_{Vr} = 1 as a default for all figures except for Fig. 2.

Also the parameter Dark Fermi level Def_0 has to be extended by equation (3), which we determined empirically and fitted based on extensive measurement data of TFT devices in the channel length range from 5 μm to 50 μm.

$$Def_0 = \left(\frac{L - L_{min}}{1\,\mu m}\right) \times a + b\,, \quad (3)$$

where a, b and L_{min} are fitting parameter, which are given in Table I.

The drain and source contact resistance of a-IGZO TFTs significantly impacts device performance. Simulation accuracy is improved by extending parameters R_d and R_s of the standard RPI-aTFT model by the following equation:

$$R_d = R_s = 500\Omega \times \frac{W_{REF}}{W}\,, \quad (4)$$

where W is the channel width and the 500 Ω are technology specific.

We extend the parasitic gate-source (C_{gso}) and the parasitic gate-drain (C_{gdo}) capacitances of the standard RPI-aTFT model by a step function. Below the threshold voltage V_{th} the capacitances have their off-value Eq. (5), above they have their on-value Eq. (6):

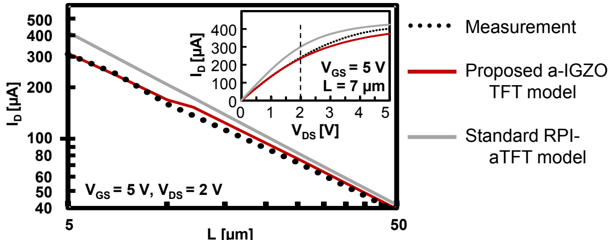


Fig. 3. Measured and fitted I_D vs. channel length L at a constant channel width W of 50 µm for V_{DS}=2 V and V_{GS}=5 V.

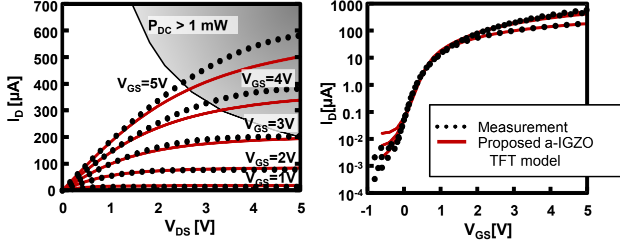


Fig. 4. Measured and simulated I_D-V_{DS} (left) and I_D-V_{GS} (right) characteristics of the a-IGZO TFT with channel width W = 50 µm and length L = 5 µm.

$$C_{gso} = C_{gdo} = L_{OV} \times W \times C_{OX} \quad , \text{for } V_{GS} \leq V_{th} \qquad (5)$$

$$C_{gso} = C_{gdo} = L_{OV} + L \times W \times C_{OX} \quad , \text{for } V_{GS} \geq V_{th} \ , \qquad (6)$$

where L_{ov} is the gate-source or gate-drain overlap length, which is 5 µm for the a-IGZO TFT technology, and C_{ox} is the oxide capacitance, which we extracted from S-parameter measurements with DC-offset.

Figs. 2, 3, 4, and 5 compare the proposed a-IGZO TFT model to device measurements. Fig. 3 also compares to a fitted standard RPI-aTFT model. Fig. 2 shows that the threshold voltage given by our a-IGZO TFT model resembles the actual threshold voltage of the a-IGZO TFT devices well, within the relevant channel-length range from 5 µm to 50 µm. It also shows the influence of process variation parameter P_{Vr}. Fig. 3 shows that the drain current I_D in the ohmic and saturation region is predicted more precisely thanks to our presented extensions of the device model. Fig. 4 shows the I_D-V_{DS} and I_D-V_{GS} characteristics for a short a-IGZO TFT. The accuracy of the new model is very good in the transition region from linear to saturation region (knee), which is important for analog circuit design. Fig. 4 also reveals that we put more emphasis on accurate fitting for V_{GS} = 3 V and below, because this area of operation is usually more relevant in analog circuits. Improving the fitting for V_{GS} > 3 V would reduce the accuracy in the remaining regions. Additionally, a power dissipation of P_{DC} > 1 mW may overheat the TFT device, which should be avoided in circuits. Fig. 5 compares AC measurements, acquired with a vector network analyzer, to simulation results for an a-IGZO TFT device of dimensions {W, L} = {50 µm, 5 µm} and V_{DS}=V_{GS}=3 V (i.e. on-state). This measurement setup requires the usage of bias tees, which limit the frequency range to 1 MHz and above. We carefully fitted Y_{11}, Y_{21}, and Y_{12}. Consequently they show very good agreements between measurement and modelling. As a trade-off, the fitting of the small-signal output admittance Y_{22} does not achieve the same accuracy. We chose this trade-off, because the overestimation of Y_{22} does not impact circuit simulation accuracy in many practical cases, for example in all cases where high impedance bridging is used between stages.

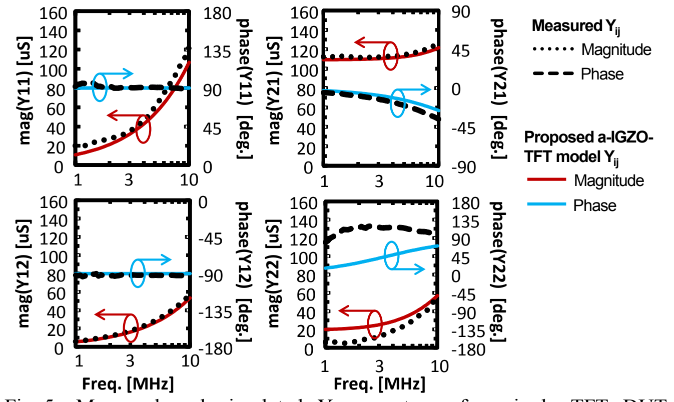


Fig. 5. Measured and simulated Y-parameters of a single TFT DUT (50 µm/ 5 µm) at V_{DS}=3V and V_{GS}=3V.

III. Experimental Results and Discussion

To validate the accuracy of the proposed model for the a-IGZO TFT technology, the Cherry-Hooper amplifier shown in Figs. 6 and 7, which is similar to [16], has been designed. The circuit is fabricated on a flexible 50 µm-thick polyimide substrate using an a-IGZO technology [2] in a chip area of 13.3 mm^2. Characterization was carried out using an oscilloscope, a signal generator and a vector network analyzer. All time domain measurements were carried out with a load impedance of Z_L = 10 MΩ ‖ 1 pF. The supply voltage for the amplifier was V_{DD} = 6 V.

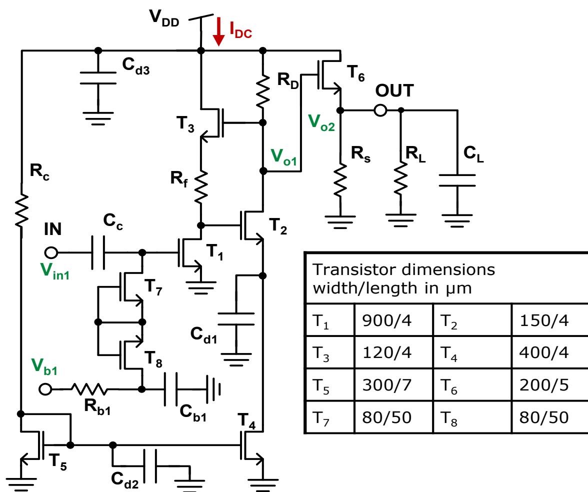
The frequency response of the amplifier is shown in Fig. 8, where measurement and simulation with our proposed model are compared. A voltage gain of 9.5 dB is achieved over a -3 dB bandwidth of 2.4 MHz, with GBW of 7.2 MHz and a DC power consumption of 6 mW. The measured drop in voltage gain below 40 kHz is caused by the AC coupling C_C of the input and by the AC coupling of the measurement setup.

Apart from this discrepancy below 40 kHz, which is expected, the simulation using our new a-IGZO TFT model predicts the actual behavior of the Cherry-Hooper amplifier well. The simulated voltage gain is between 10.4 dB and 11.2 dB over a -3 dB bandwidth of 2.1 MHz. The predicted gain is above the measured, which is expected because the simulation does not include parasitics. The simulated GBW is 7.0 MHz and differs from the measured GBW by only 0.2 MHz.

To verify the accuracy of the proposed a-IGZO TFT model for predicting nonlinear behavior of the circuit, we compared the simulated and measured dynamic output range of the Cherry-Hooper amplifier. The measured 1 dB compression point of the amplifier is -7.5 dBV (0 dBV=2.828 V_{pp}) and differs from the simulated 1 dB compression point of -8.5 dBV by only 1 dB.

IV. Conclusion

A compact model for a-IGZO TFTs and its application was presented in this paper. This model builds on the RPI-aTFT model (Rensselaer Polytechnic Institute model for amorphous silicon TFT). We improved over this standard RPI-aTFT model by adding equations and parameters to enhance the prediction accuracy for a-IGZO TFTs. We also used binning to enable the modelling of the non-monotonic channel length dependent threshold voltage of the a-IGZO TFTs. Our model provides scalability in drain current, extrinsic overlap capacitances, and a drain/source contact resistance of the a-IGZO TFT devices.



Transistor dimensions width/length in µm

T_1	900/4	T_2	150/4
T_3	120/4	T_4	400/4
T_5	300/7	T_6	200/5
T_7	80/50	T_8	80/50

Fig. 6. Schematic of the Cherry-Hooper amplifier including output buffer T_6.

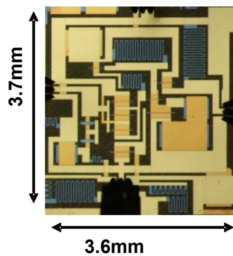


Fig. 7. Die photo of fabricated flexible Cherry-Hooper amplifier.

The practicality and the accuracy of the proposed a-IGZO TFT model were validated by comparison of simulations and measurements of a Cherry-Hooper amplifier, which was implemented in a-IGZO TFT technology and subsequently characterized. The model was fitted to the technology based on large sets of measurements for channel lengths ranging from 5 µm to 50 µm. However, the validation of the model showed that the model can also be used for shorter channel lengths. The Cherry-Hooper amplifier was implemented using devices with a channel length of 4 µm. We have also compared simulated and measured non-linear behavior, and provided means to handle process variation induced threshold voltage variations during simulation.

In summary, this work presented a new compact thin-film transistor model and its application for a-IGZO TFT devices and circuits. The resulting new a-IGZO TFT model is a behavioral model that increases the range of operation and provides improved simulation accuracy.

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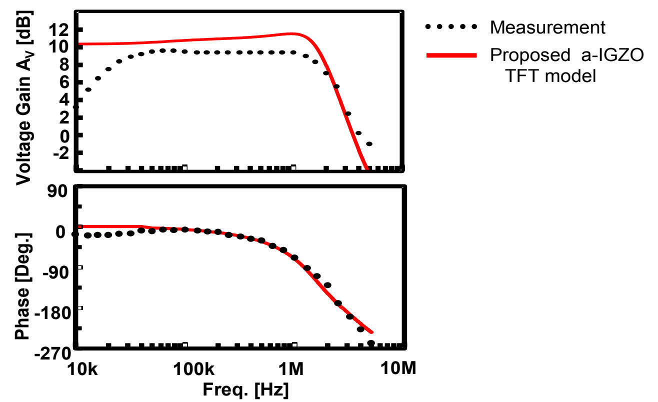

Fig. 8. Comparison of measured and simulated frequency response of the Cherry-Hooper amplifier.

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